# Si recoil detectors + FEE

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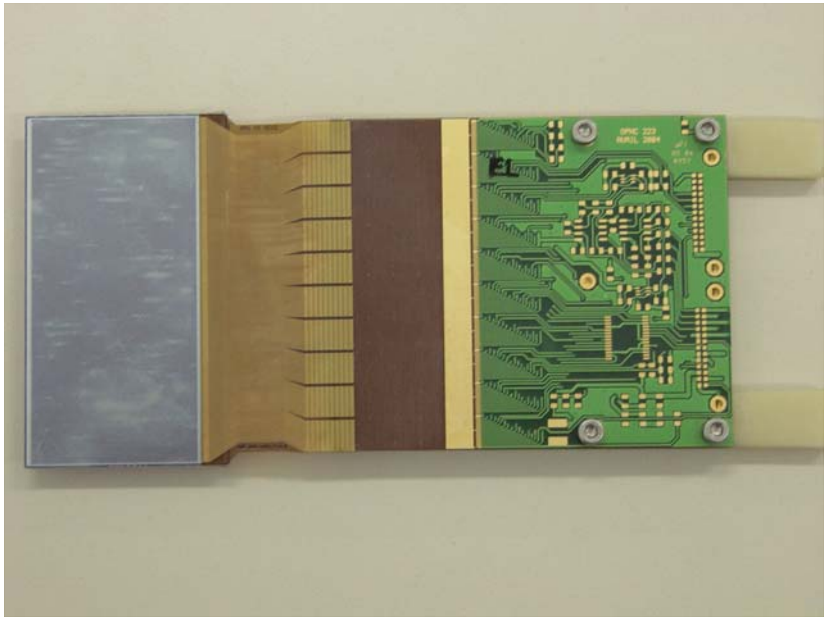
# Detector types

- Double-sided Si microstrip detectors (R3B and EXL) – 100 μm and 300 μm thick, 100 μm and 300 μm strip pitch, partly backeable – many different types
- SiLis (EXL) – 8-9 mm thick, 9 x 9 $cm^2$
- Many different types are necessarily, all with high ΔE precision

# Si microstrip detector prototypes (AMS-type)

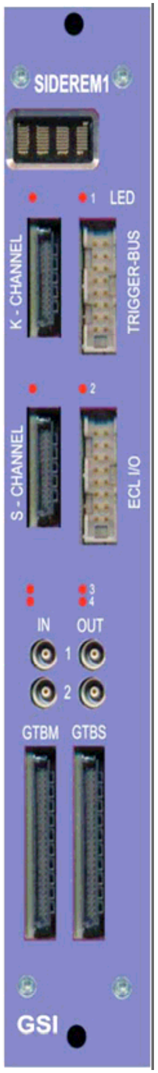
DSSDs, 300 $\mu$m thick, 41 × 72 $mm^2$
Strip pitch 100 $\mu$m
High dynamic range
1024 readout channels/detector
Designed to work in vacuum (total power dissipation < 3 W/detector)



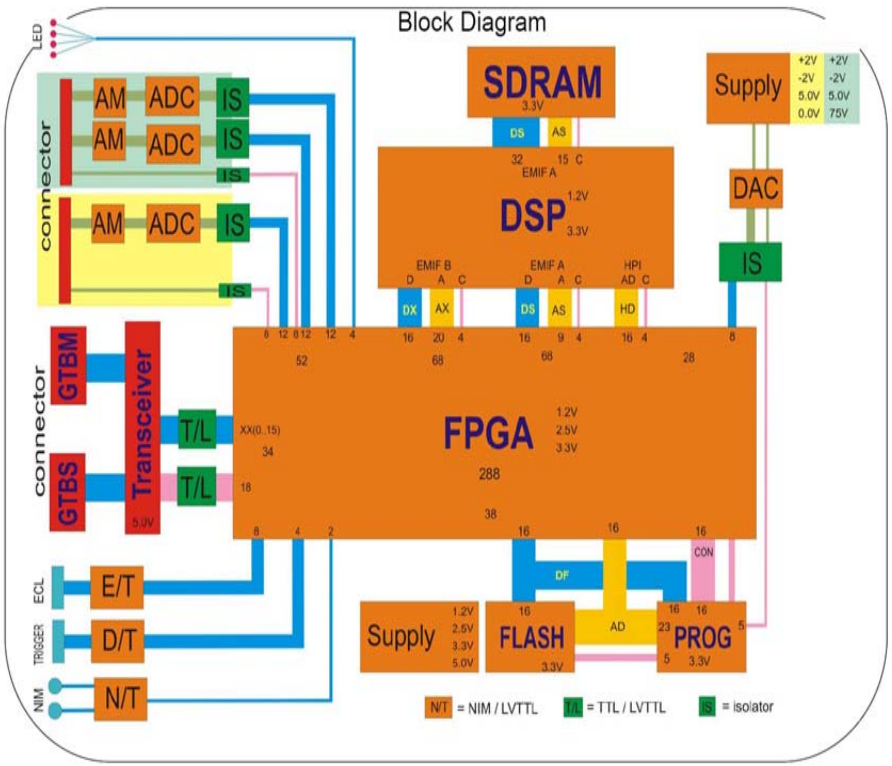
9 detectors + FEE boards are available

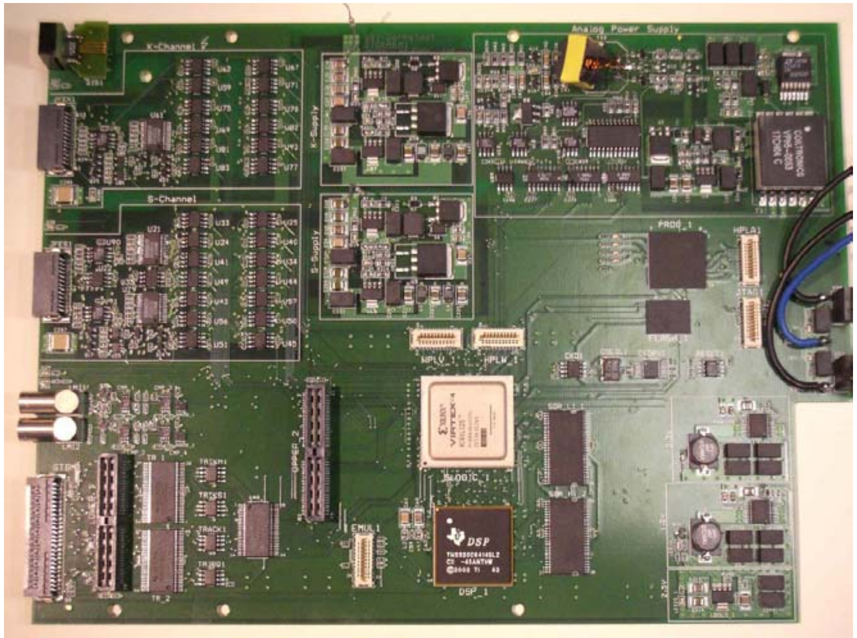
# GSI digitizing board SIDEREM

- Silicon Detector REadout Module (SIDEREM) – 3 fast 12 bit ADCs, pedestal suppression, processing by DSP
- Board has a slow control features – setting/reading of a bias and conversion time, reading a temperature
- Connection from detector via two special cables
- Conversion + processing time ~ 100 μs $\Rightarrow$ maximum rate $10^4$ events/s



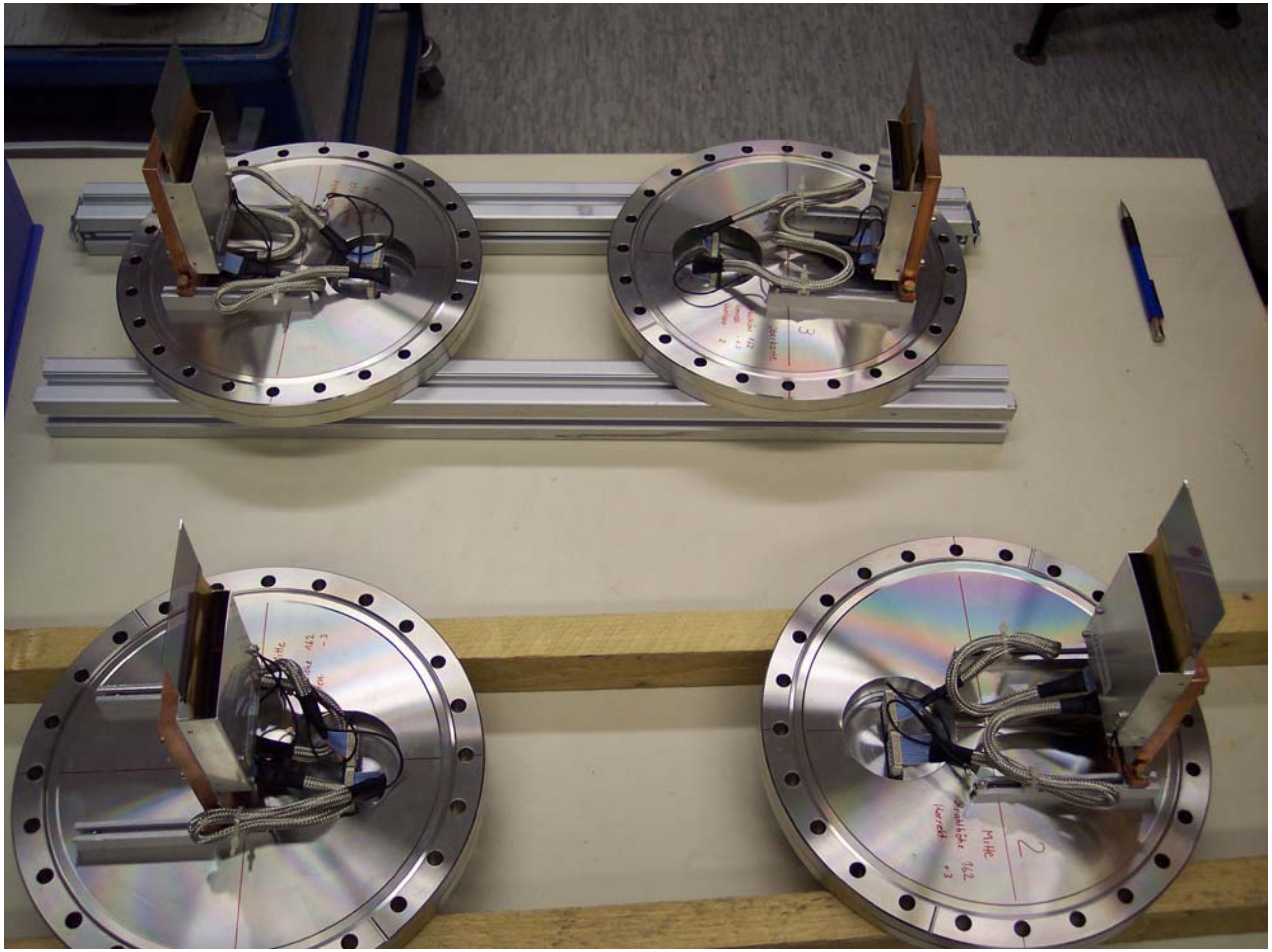
# GSI digitizing board SIDEREM



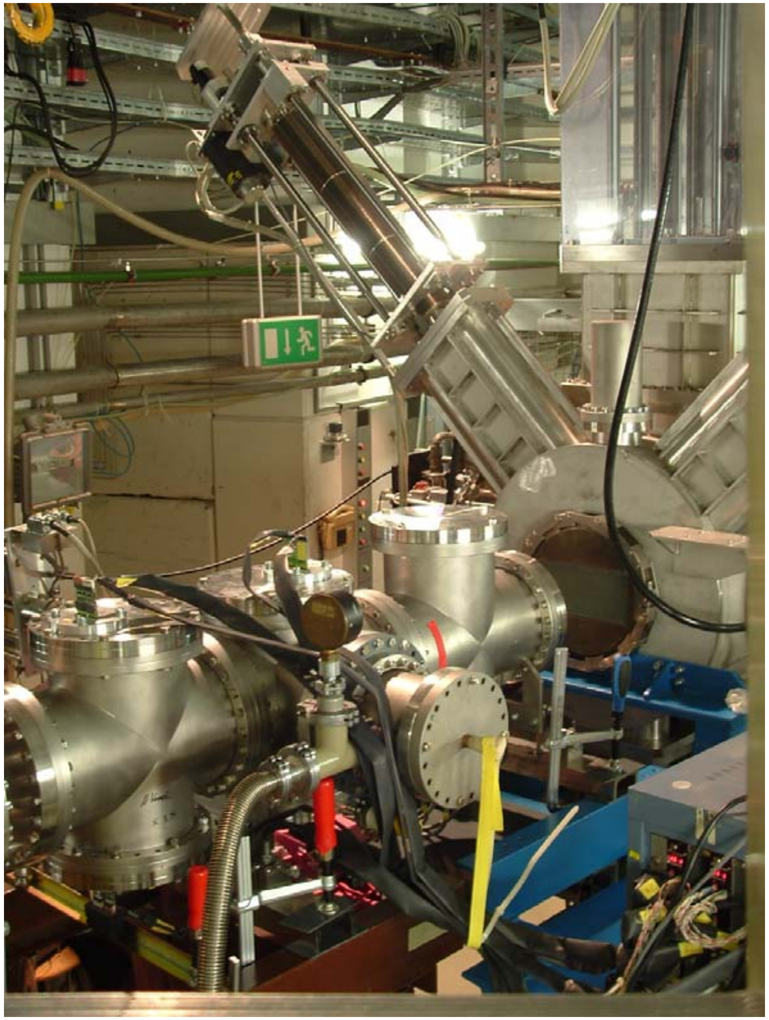
Up to 15 detectors could be readout by SIDEREMs and single SAM module
All modules and SAM are connected by GTB interface (data rate up to 5 Mb/s)

# Four prototypes

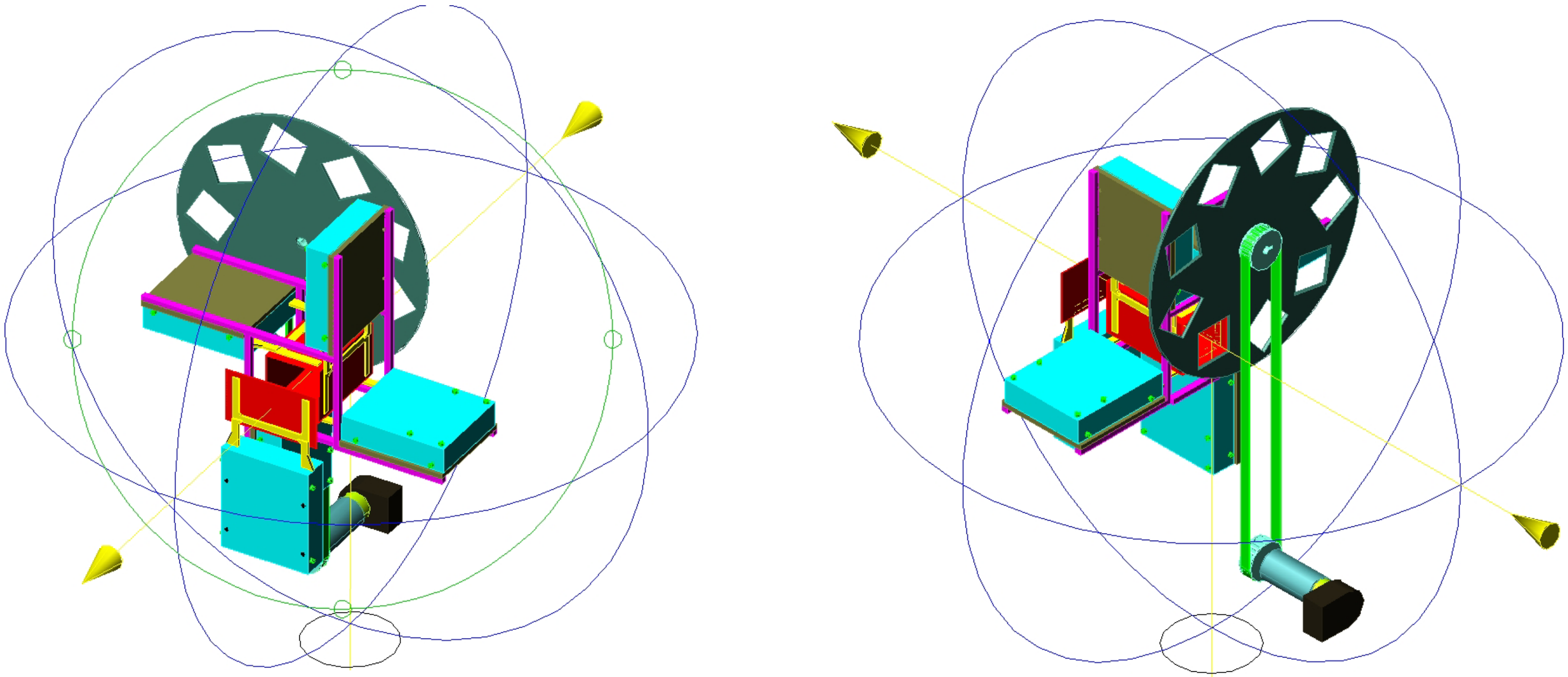


# Experiment S271 at FRS

- $^{19}$Mg -> $^{17}$Ne + 2p at FRS, August 2006
- 4 detectors were installed into beam line
- Part of the FRS setup
- Successfully detected heavy ions and protons
- Tested with the trigger rate up to 7 kHz



# New experiments with AMS-type detectors



10 more SIDEREMs will be produced soon

6 Si detectors will be tested inside a Cristall Ball – 20-21 November 2006

Will be used for few experiments: $^{12}C$ and $^{40}Ca$ QFS, $^{17}Ne$ knock-out, $^{23}Al$ Coulomb dissociation, $^{32,34}Ar$ giant resonance experiments in Cave C during 2007-2008

# MUST2 DSSDs

- CEA/Saclay - 5 detectors, 300µm, 10 x 10 $cm^2$ with 2 µm thick Al window, from MICRON
- 4 similar detectors with thin (150 nm) window and with a thick window at the backside, from MICRON
- Detectors should be available and tested in October-November 2006.
- Could be tested at the ESR in 2007.
  But -MUST electronics is not bakeable

# Thin DSSD (MICRON)

- AC Coupled DSSD
- Active Area: 52 mm x 67 mm
- P-Side - 512 strips (pitch 102 µm)
- N-Side - 316 strips (pitch 214 µm)
- Both sides with a charge division with intermediate strips
- Coupling Capacitors: 200pF P Side / 400pF N Side
- Bias Resistors: 12M
- Thickness: 100µm
- GSI ordered (in 2005) one detector, supposed to be used for ESR tests
- But – problems with wafers, unpredictable timescale
- Another options – SINTEF (Norway), others?

# DSSDs from PTI

Semiconductor Lab of PTI, St. Petersburg started a design of few new prototypes:

a) DSSD 300 μm thick, 2 x 2 $cm^2$, 300 (100) μm strips

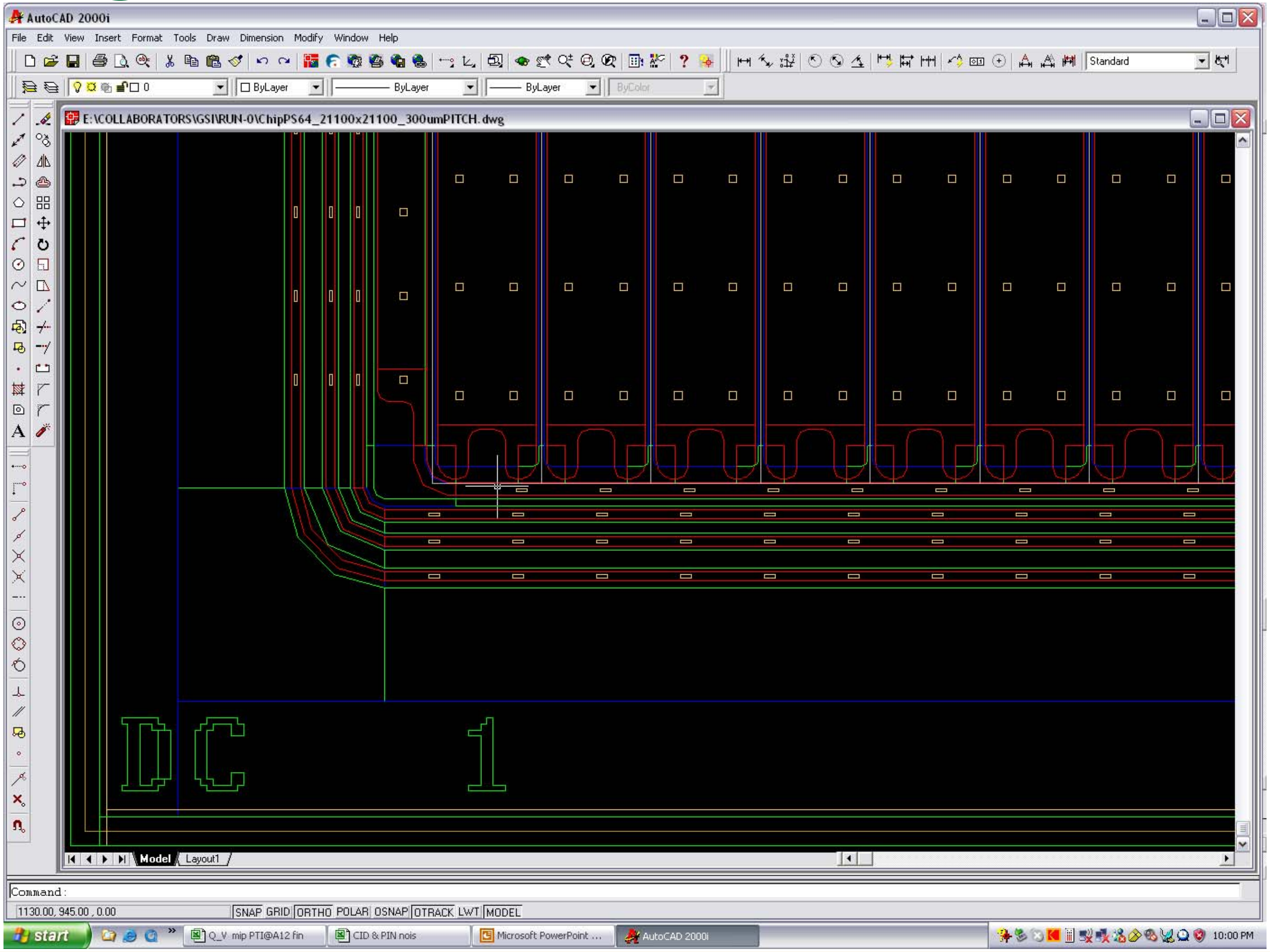
b) DSSD 150 μm thick, 2 x 2 $cm^2$, 300 (100) μm strips

Time scale – 5-6 months

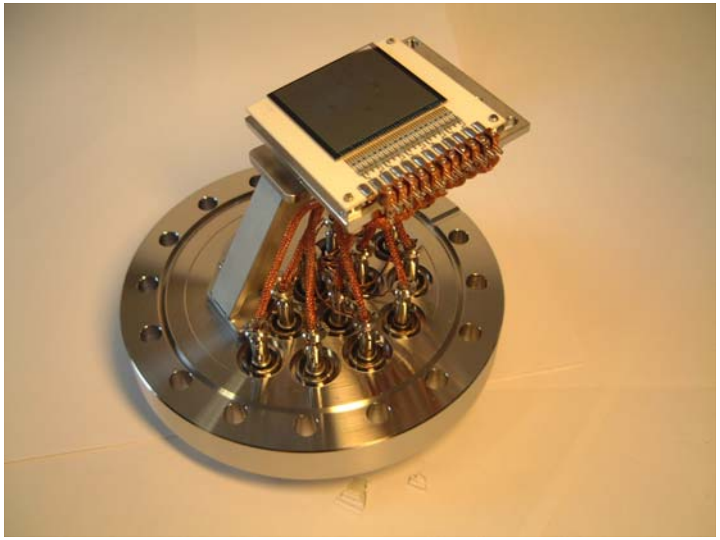
Readout: chips – FREDA (RAL/Daresbury), readout boards (Daresbury)

Could be tested at GSI or KVI

# Design of DSSD at PTI



# UHV compatible Si SSDs



active area: 40 x 40 mm², thickness: 1 mm, UHV compatible

1 μm Ni foil in front to protect from UV light and electrons

40 strips 1 mm wide are connected via resistors into 5 groups

One detector is tested in lab and at ESR conditions
Last measurement – December 2005, EXL feasibility test
Elastic $^{136}$Xe(p,p) cross section measured with it's help
One more detector is available

New project – Si or diamond position sensitive detectors in the vacuum pocket and in UHV for ion's tagging, size – 6 x 6(10) cm$^2$

# SiLi detector prototypes

Semiconductor Detector Lab, PNPI, St. Petersburg with many years experience in production of planar SiLis;

desing of the prototypes started (5 mm thick, size to 5×5 $cm^2$), with pads, small dead zones on edges, UHV compatible is still a question

Time scale - end of 2006

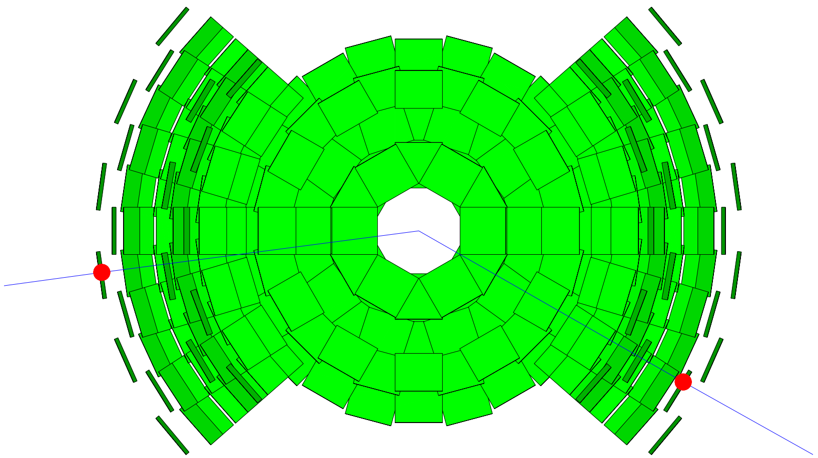
Could be tested at PNPI using an $\alpha$–source and protons 200-1000 MeV, then at GSI

Jülich makes 2 detectors 6.5 mm thick (MUST 2 type), area of 9 x 5 $cm^2$ , with pads, construction is UHV capable (on ceramics). Tests started, $\Delta E \leq 50$ keV achived.

Time scale - November 2006

# Simulation and optimization

- tools - Geant4+ROOT
- recoil Si detectors + calorimeter, individual crystals + Si detectors
- no frames and infrastructure yet
- interface to event generators
- CAD design of R3B recoil system is needed

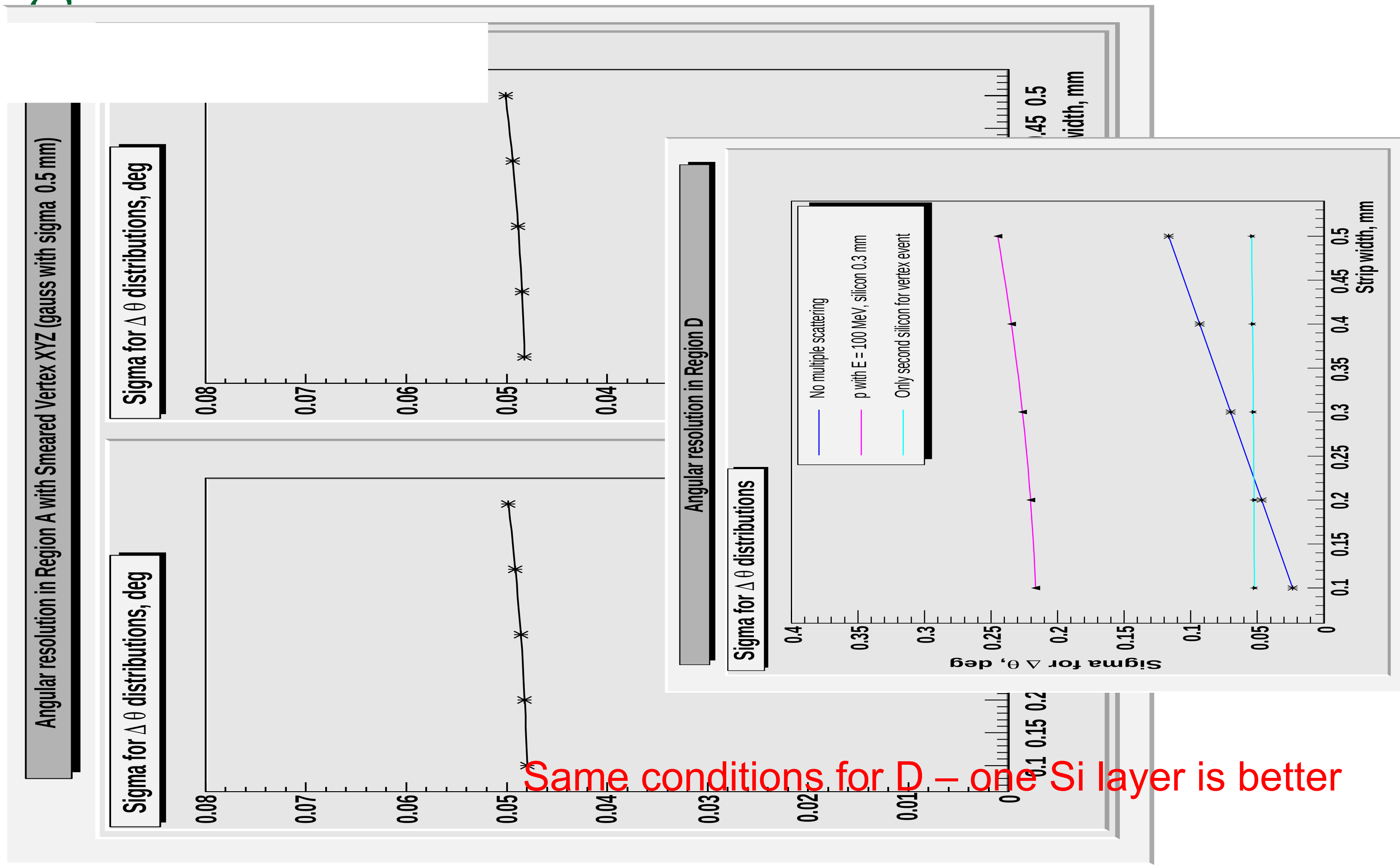


EXL recoil detector

# Optimization parameters

- **The main sources which define angular resolution:**
  - silicon strip width,
  - distance from the event vertex to the silicon,
  - vertex position uncertainty.
- **In case of two layers (regions D and C) it also depends on:**
  - multiple scattering,
  - distance between two layers.

# Angular resolution




Same conditions for D – one Si layer is better

Beam 0.5 mm + target 0.5 mm ⇒ no difference between 0.1 and 0.5 mm strips

# INTAS

**INTAS Collaborative Call with GSI – March 2006**

**Proposal “Development of Double-Sided Silicon Microstrip and Li Drifted Silicon Detectors for projects EXL and R3B” submitted in May 2006**

**Participants - PTI, St. Petersburg, RIMST, Moscow, PNPI, St. Petersburg, GSI, Uni Mainz, Daresbury; coordinator – O. Kiselev**

**Total budget – 100 k€ for 2007-2008**

**Positively evaluated by experts in August 2006, final decision – October 2006**

**In total ~20 proposals, only one from NUSTAR and unfortunately rejected by INTAS due to too small budget and too short time for an ambitious project**

# BARC, India

- **Experience – 1000 single-sided detectors using 300 µm wafers and ceramic frames for CMS assembled and tested**
- **Official letter about participation in R3B/EXL**
- **Can try to produce DSSDs, interested in FEE and ASIC design**
- **Technical requirements for the detectors and responsibility need to be defined**

# Responsibility

- Liverpool: Facilities for bonding (only for mass production), detector testing are available, good connection to MICRON
- Saclay: Setting up and testing of prototypes
- GSI: Detector tests without and with a beam, detector baking, test of outgasing, etc…
- PTI St. Petersburg: Production of masks, mass production of chips, detector tests
- Others???

# Front-end electronics

- IDEAS chips for 50-200 µm strips, 5 MHz/10 MHz clock, not backable PCBs, very low power (0.3 mW/ch) consumption, no timing, SIDEREM/SAM boards with 12 bit ADCs and DSPs
- MUST2 chips for 782 µm strips, 2 MHz clock, not backable PCBs, high power consumption, 0.5 ns (leading edge) time resolution, MUVI readout with14 bit ADCs
- RAL/Darebury FREDA chips for 200 µm strips, boards with 12 bit ADCs - already available, flexible design

# WG meetings

- Regularly twice per year
- Previous meeting – 26-27 April 2006 in Liverpool with participants from SPIRAL2 group (Saclay)
- Last one – 3-4 October 2006 in Milano
- Next – building the ‘demonstrators’, coupling of DSSDs to CsI crystals and beam tests