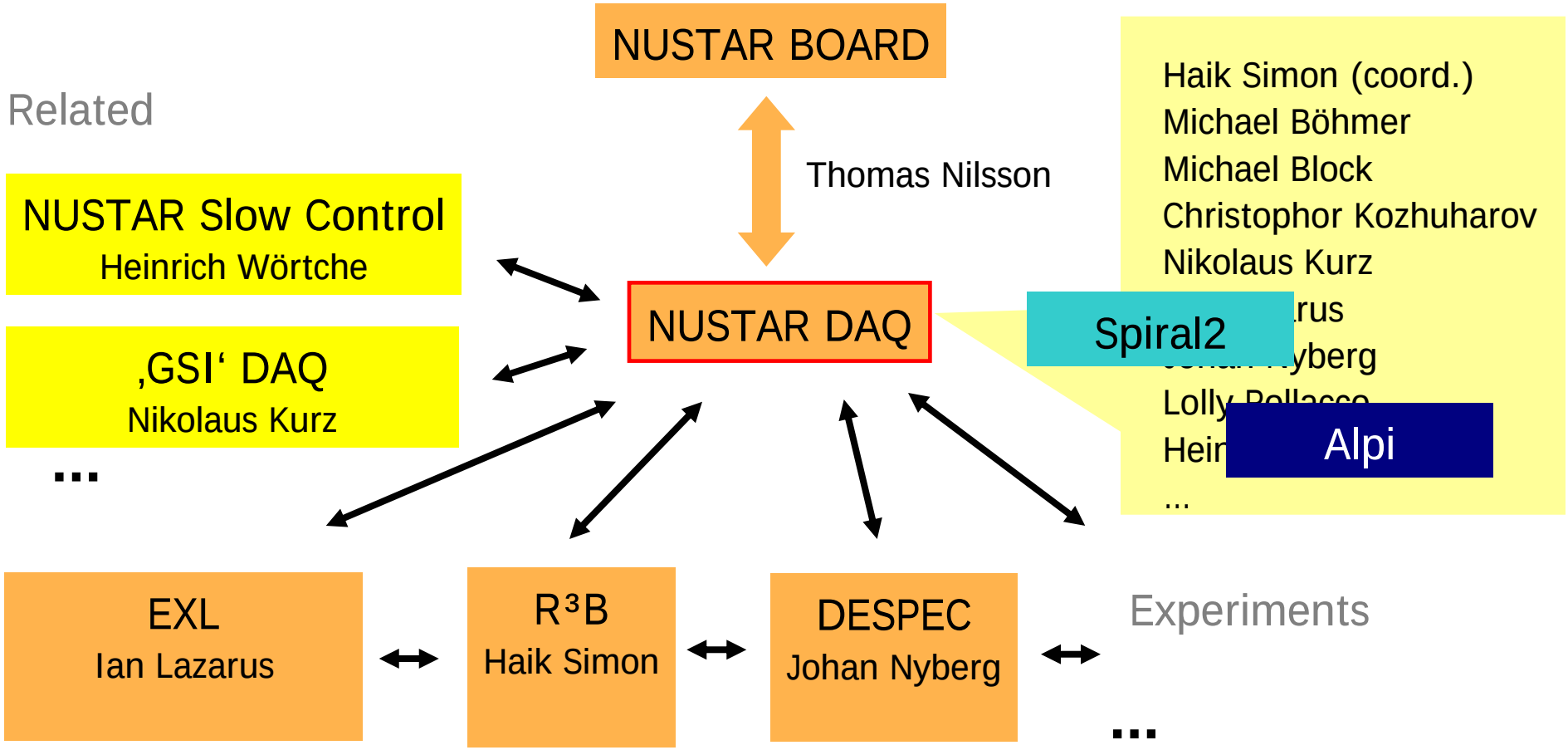
NUSTAR DAQ/FEE organisation



NUSTAR-DAQ/FEE scope

i. Integration

- FAIR Infrastructure
- Interconnection with other detection & DAQ systems

ii. Standardisation, Flexibility

- couple different standalone “NUSTAR” DAQs
- interconnects for triggers and control signals
- modularity of the system
  (local triggers / event buffer capabilities / timestamps)
  → Ian Lazarus‘ report

iii. Standardisation, Synergies

- frontend electronics & digitization
- ASICS

→ Interface definition .

NUSTAR DAQ/FEE WG

2004 Initial Meeting

2005 R³B/EXL workshop
FEE FAIR workshop (CBM, panda, NUSTAR)

2006 NUSTAR/SPIRAL2 → 3 annual Meetings
/2007 (GANIL, GSI, Italy, KVI)
2nd FEE/DAQ FAIR workshop (CBM, panda, NUSTAR)

System design for i & ii:

- data-transfer docking stations (station A)
- slow-control docking stations (station B) and
- time-synchronization docking (station C) station

GSI FAIR

Data-transfer docking stations (station A)

- data collection from detector systems (N × M)
- transfer and event building
  - Interface to second level trigger processor farm
  - Interface to online analysis
  - Interface to slow control systems
  - …
- storage

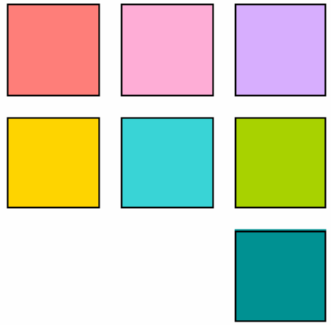
Slow-control docking stations (station B)

- checking hardware structure
- system initialisation
- providing (bi-directional) system parameters (data bank, slow control events)
- system monitoring
  - scalers
  - digital signals (soft scope)
  - analogue signals
  - subsystem timing
- safety

slow-control docking stations (station B)

H. Wörtche, H.S

1. checking setup (hardware, systems)
2. system initialisation
3. system parameter setting
4. monitoring (analog/digital) and safety
   → DAQ, Interlocks

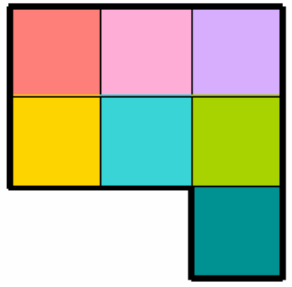


→ Hierarchy

- local controllers (hardware access, sub systems, acc. slow control …)
  system integration: functionality / interface description
- global docking station

→ Database (flexible building blocks)

i. representation of the component (GUI, synoptic, …)
ii. coordinate in the detector setup
iii. definition of the parameters
iv. model: dependencies, limits, safety conditions, status
v. software revisions



Time-synchronization docking (station C)

BuTiS: Bunchphase Timing System

- Standard frequencies: 100 kHz, 10 MHz, 76 MHz(PHELIX),
  155,52MHz(OC-3, network std.),
  200 MHz

- Absolute time stamps

- Precision better 100 ps / km

Optical fiber system, receiver cost high:
→ one receiver/ cave, local time distribution system

iii. Standardisation, Synergies Status

- ASIC design
  - Expert groups identified:
    Daresbury, Saclay, Lund
    EXL/Spiral2 (Silicon)
  - GSI timing applications

    → interest and specifications should be expressed and provided now !

- Resource planning for IT Infrastructure

  → Input needed: storage capacity
  compute farms
  …

Status (spring/2006)

Data transfer (station A):

- system architecture still under discussion
- available man power limited
- startup (?)

Slow Control (station B):

- system definition depends on A
- task allocated to KVI
- startup 2007 (if not delayed by A)

Timing System (station C):

- active BuTiS development for and by accelerator
- local time distribution architecture unclear

Differential Status

Data transfer (station A):

- system architecture still under discussion → Narval, MBS, (?)
- available man power limited → Synergy with GANIL & KVI

→ Negotiations with Coburg university of applied sciences

(1) Dep. of Electrical engineering/Computer science
Master student VHDL programming (10/06 -)

(2) additional Master study Program
(Analytical Instruments, Measurement and Sensor-Technology)
[joint with USST Shanghai]
(2-3 Master students end/2006 – beginning/2007)

→ NUSTAR/DAQ engineer@GSI (2007)

→ Trigger simulation via „Hochschulzusammenarbeitsvereinbarungen“ TU-Darmstadt
i.e 1 Postdoc + inv. (2007) [decision expected now]

Differential Status

Slow Control (station B):

→ concept drafted

→ acknowledged by SPIRAL2/FAIR/KVI working group coordinator

→ first contacts with data-bank experts (ORACLE) University of Groningen

→ KVI position (Software engineer to be filled by end of this year (short list exists))

→ next step: preparation technical proposal

Timing System (station C):

- active BuTiS development for and by accelerator
- local time distribution architecture unclear

→ ongoing work on building layout (~ fall/2006)

Start of specific projects:

- Demonstrators
- System Design/Helper Modules