Technology which might be useful for EXL…

- Digital Pulse Procesing
- Total Data Readout (TDR)
- AGATA

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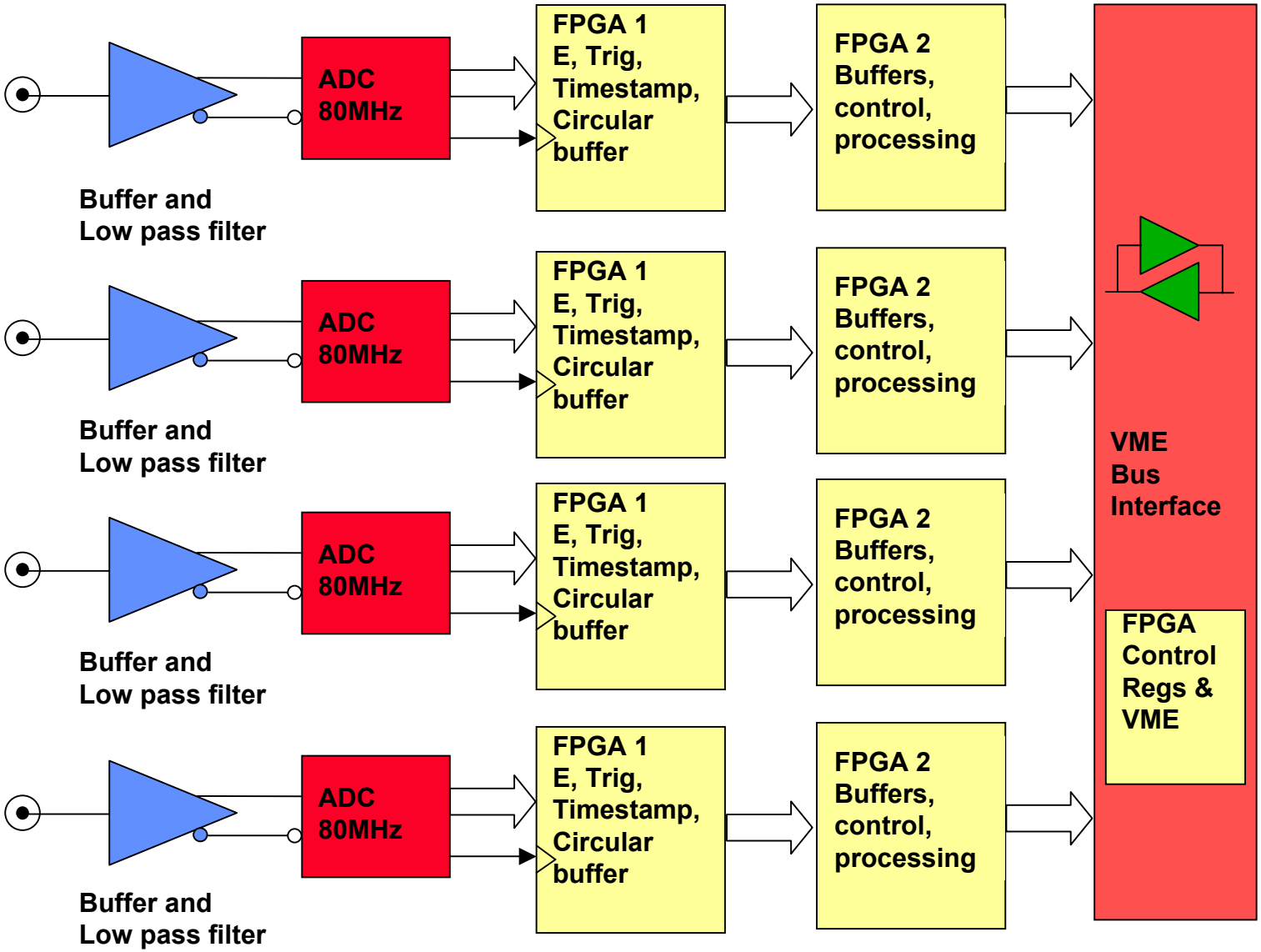
GRT4 Block Diagram



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Digital Pulse Processing

- Advantages:
  - Flexible can even change according to rate.
  - Stable (no analogue shifts (except ADC, input buffer))
  - E, T, Position, pulse discrim…

- Limitations:
  - ADC width/sampling rate *(14bits 100MHz, 10bits 1GHz)*
  - ADC power *(1.5 to 6Watts for the fastest)*
  - ADC input range *(2V pk-pk typ- 14 bits = 0.1mV lsb: beware of noise!)*
  - Not a magic solution- *need time to extract signal from noise.*

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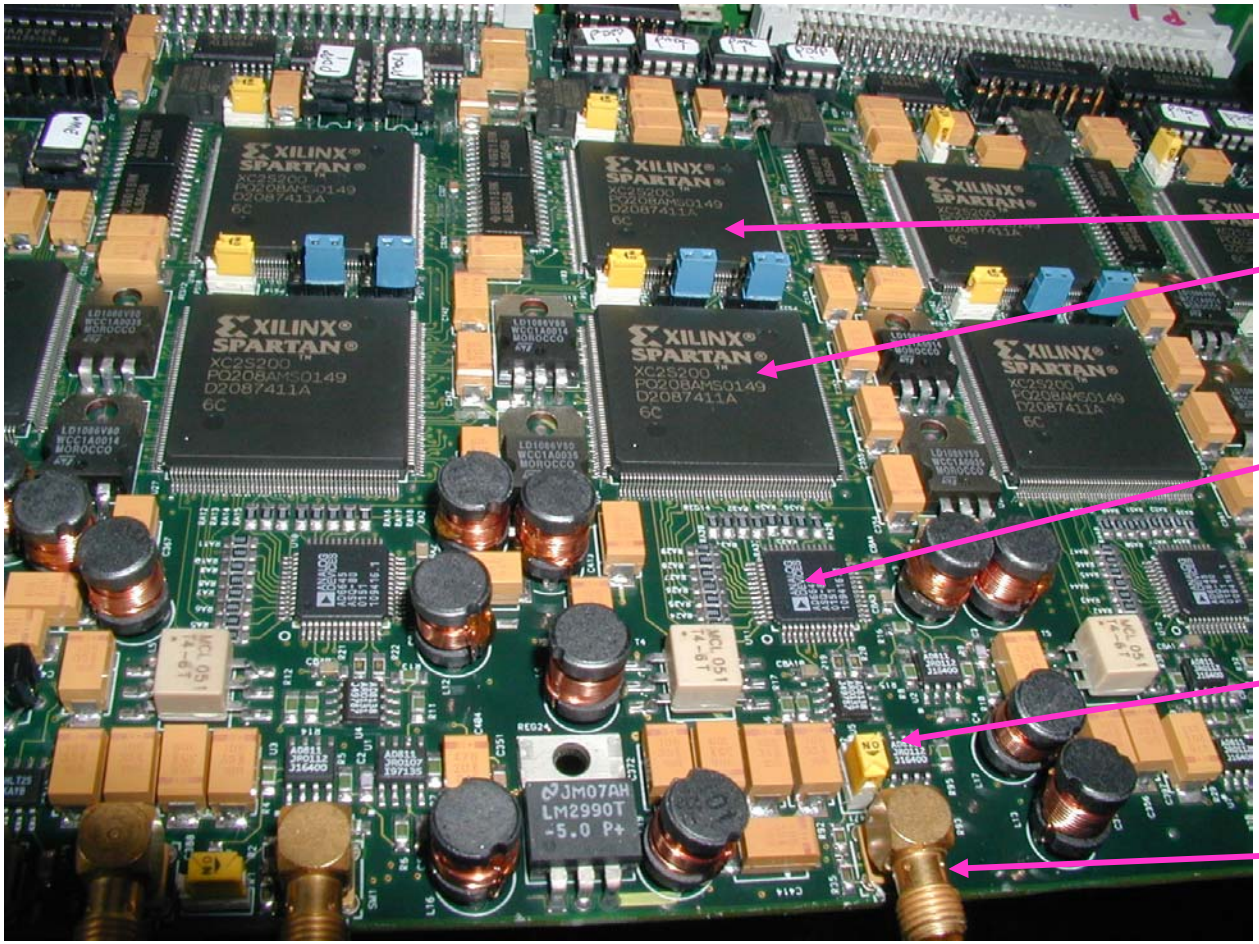
GRT4 Picture



Two FPGAs Per input (400k gates)

14 bit 80MHz AD6645 ADCs

Switchable differentiation

SMA 50ohm Inputs (4)

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GRT4 outline specification

- 4 inputs: 0-550mV into 50ohms Gain is x2
- Between input and ADC are a 40MHz bandwidth low pass filter and optional differentiator (Full scale = 15mV/ns slew.)
- ADCs are 14 bits, 80 MHz
- Trigger Input (Fast NIM)
- Busy Out (can be changed under s/w control to be used as Trigger output (Fast NIM))
- Gate In (can be used either as trigger gate or else to synchronise timestamps) (Fast NIM)

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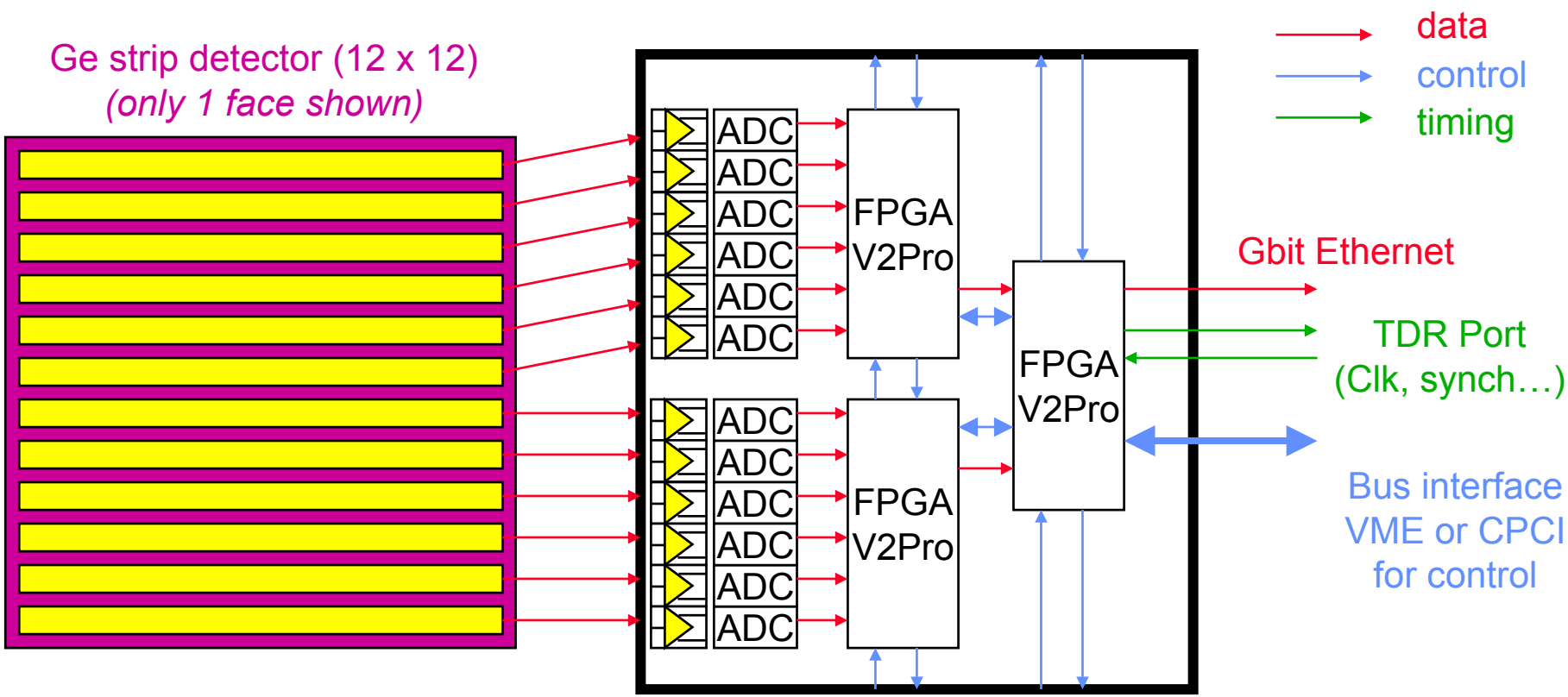
What next?



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SMARTPET electronics

- Analogue input buffer stage with gain adjust, level shift, Nyquist filter, differential output
- ADC: 14 bits 100MHz (AD6645 or ADS5500 or …?)
- FPGA: Virtex 2 Pro (e.g. 30k logic cells XC2VP30-5FG676C)
- Links to send hit patterns, trace or computed data to:
  - adjacent strips (same card or another card)
  - opposite face
  - opposite detector (PET)
- Gbit Ethernet output port: up to 100Mbytes/sec over Cat 5 twisted pair (= up to 150bytes/ADC @50kHz)
- TDR Port for synchronised counter system using Metronome:
  - Clock (100MHz or less) (in)
  - Synch pulse (in)
  - Reset (in)
  - Error (out)

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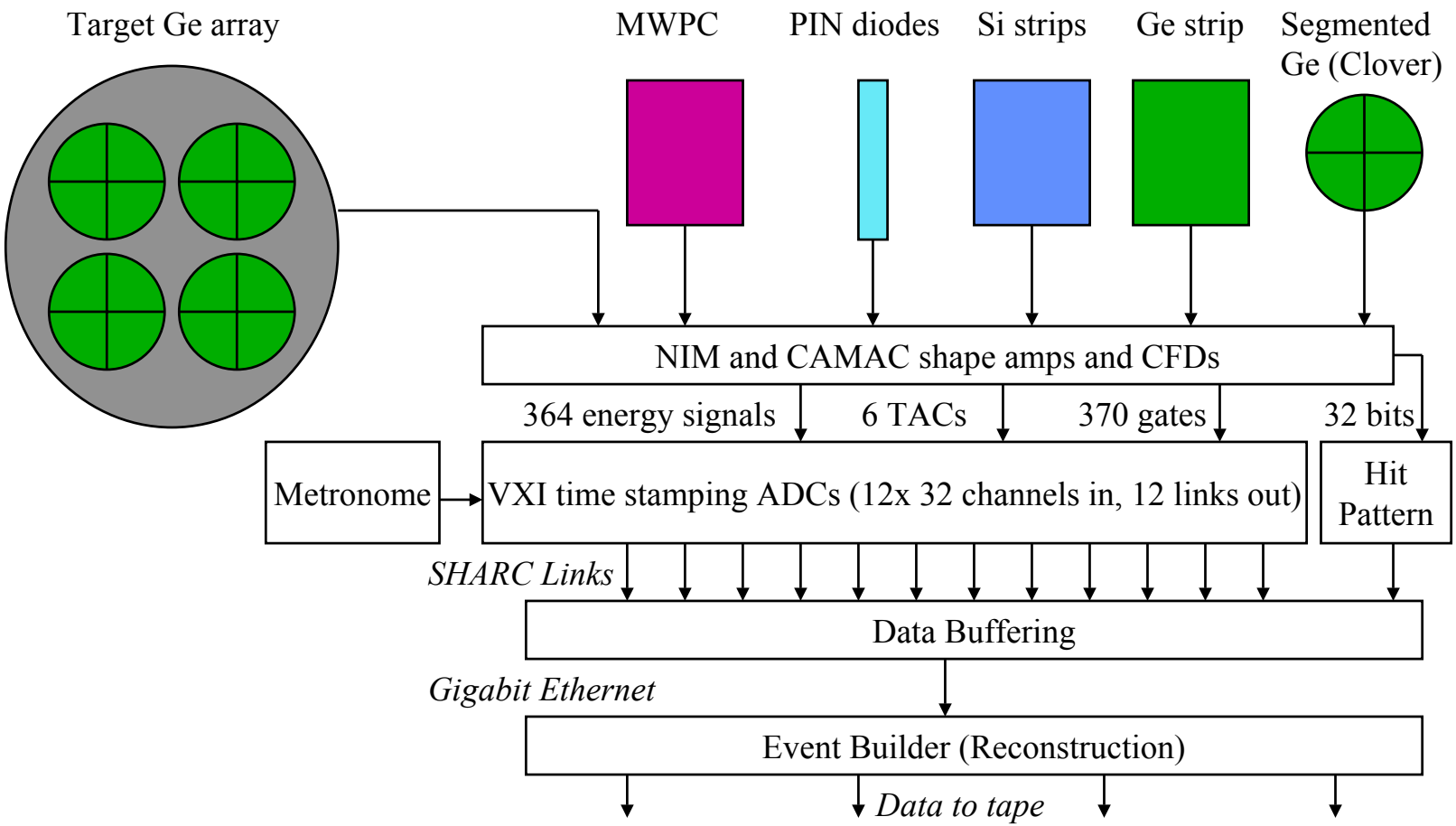
The GREAT Triggerless Total Data Readout
Conceptual block diagram



TDR Method:
Use 10ns timestamps to label data
Read it all and correlate later in software

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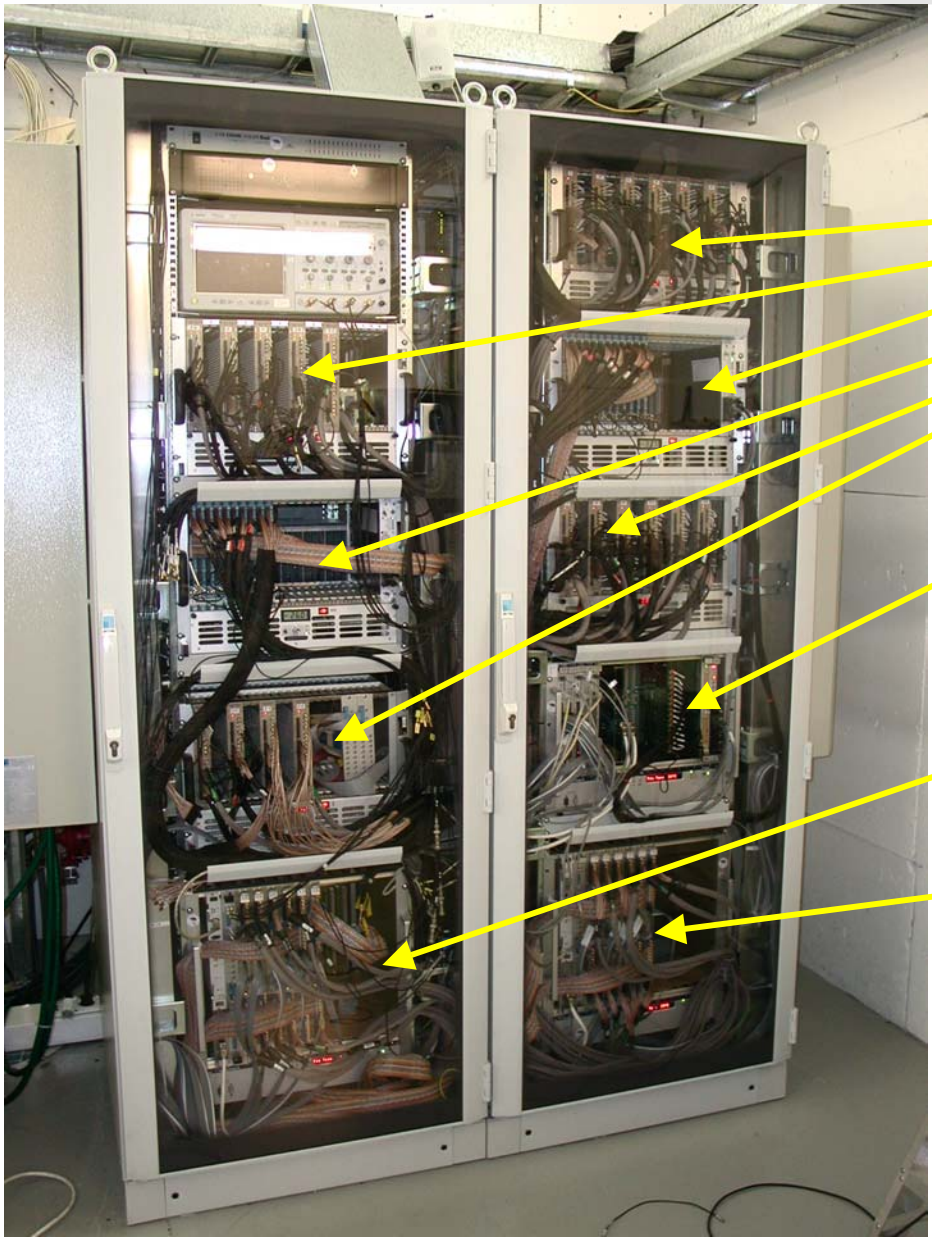
The GREAT TDR Racks in Jyvaskala



Rack includes

- 4 NIM and 2 CAMAC for front end Amps, CFDs.
- A VME crate (data merger, metronome and pattern unit)
- 2 VXI crates containing between 12 and 15 32 channel cards (up to 480 channels).

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Error detection and recovery

- System Synchronisation checking and recovery:
  - Synch pulse sent every 640us by the Metronome:
  - ADC/PU inserts “heartbeat” into data stream and checks that the local timestamp counter is correct (Auto-correction).
  - Heartbeat timestamps give a positive “no data” indication in low rate channels. Stops event builder waiting for ever.
- After power fail/software reboot
  - All local timestamps can be pre-loaded and restarted at correct value

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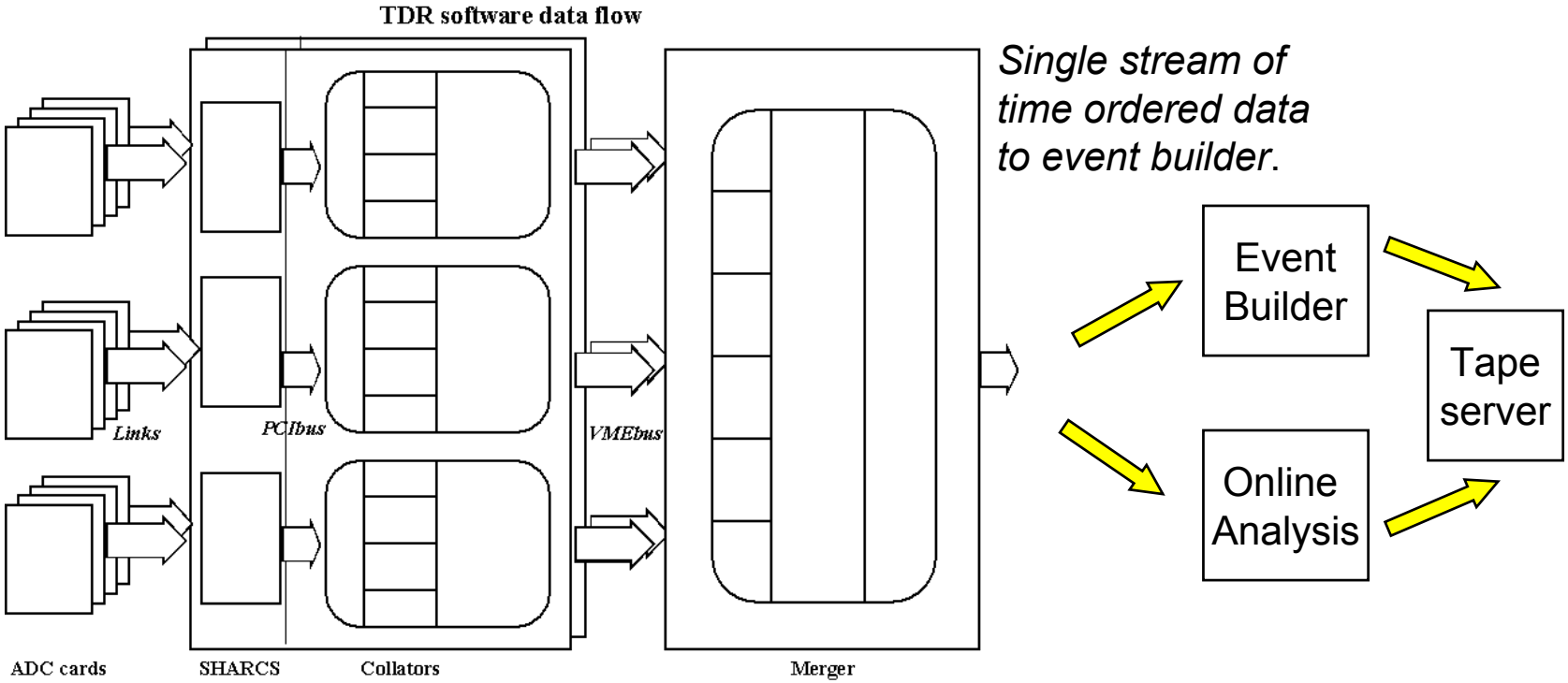
TDR Data Flow



- *Each ADC card and Pattern Unit has a SHARC link which is received by one of four 6-input SHARCs spread over 2 VME boards.*
- *The SHARCs are read inside the VME cards over an internal PCI bus into an event collator task*
- *Data are sent over VME bus to a merger task running in a VME CPU*
- *Merger sends a single stream of time ordered data on to the event builder using Gigabit Ethernet.*

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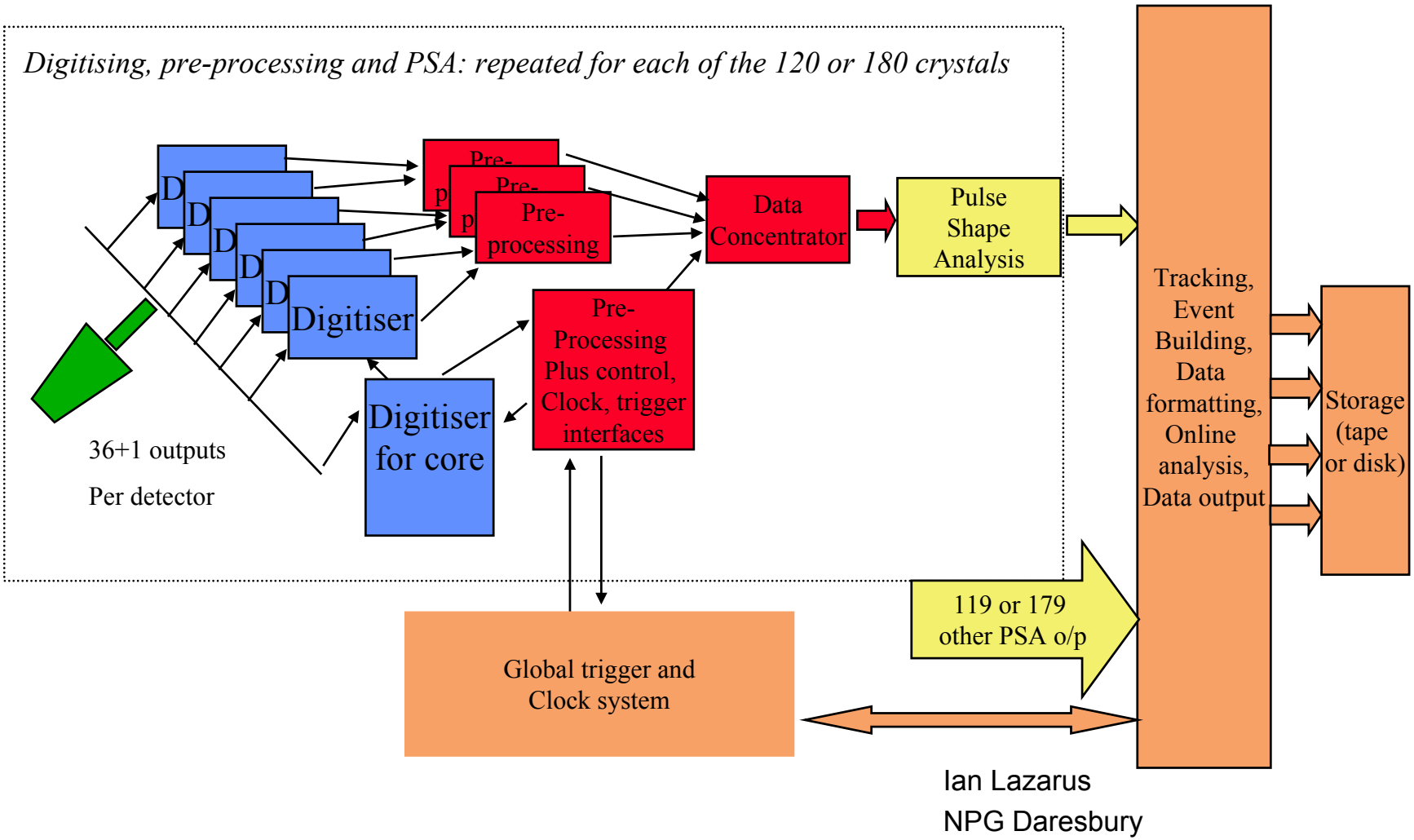
AGATA Schematic System Diagram



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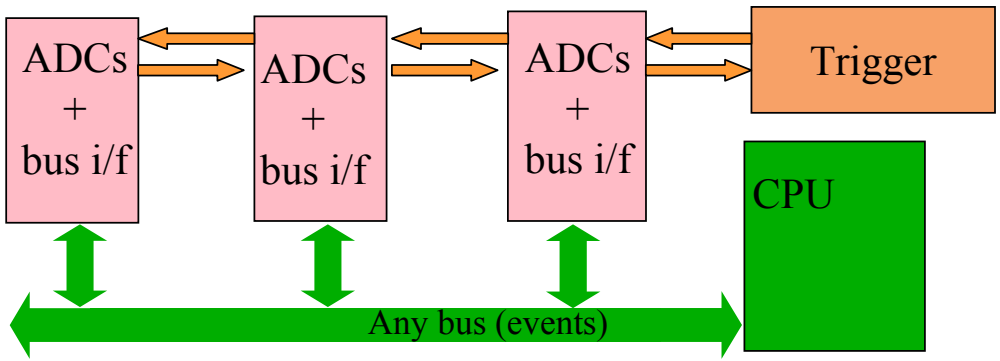
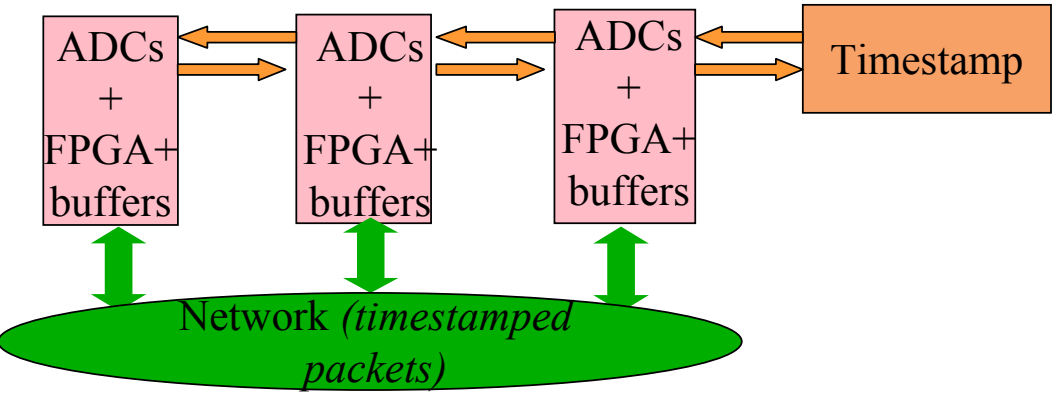
DAQ Data Flow



Conventional-

- Data collected from the bus
- Event building in hardware using event numbers.
- Limited by bus readout



Data Packets-

- Generate timestamped packets - send data buffers
- Event building in software using time stamps.
- Limited by software & CPU

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