Digital spectroscopy and coincidence timing

NuSPIN School

UNIVERSITY OF LIVERPOOL

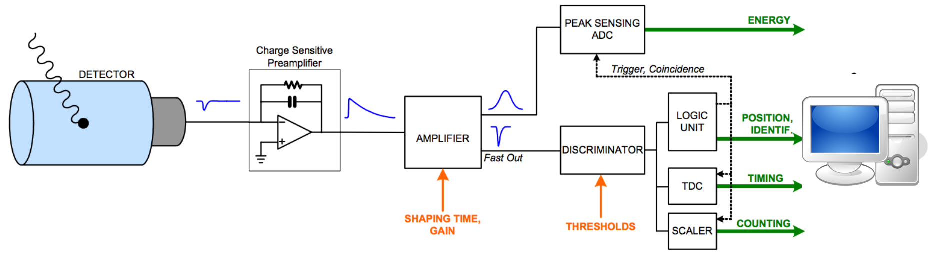
Topics

In this lecture:

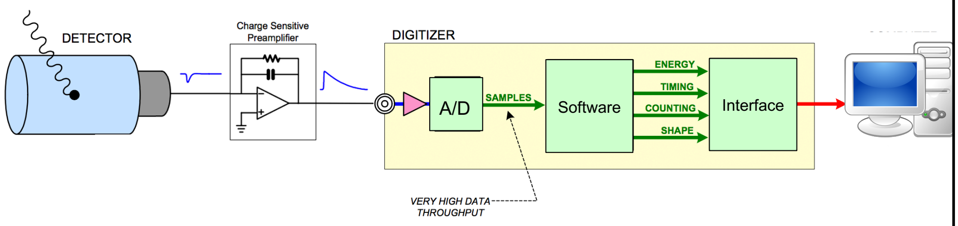
- Comparison of analogue and digital Pulse Height Analysis (PHA)
- Why digitise detector signals?
- The principles of signal digitisation
- Energy filter (Moving Window Deconvolution)
- Timing filter
- Digitiser types
- Multichannel digital systems
- Digital coincidence / TAC measurements

Digital v's analogue PHA

An analogue pulse height analysis system consists of:

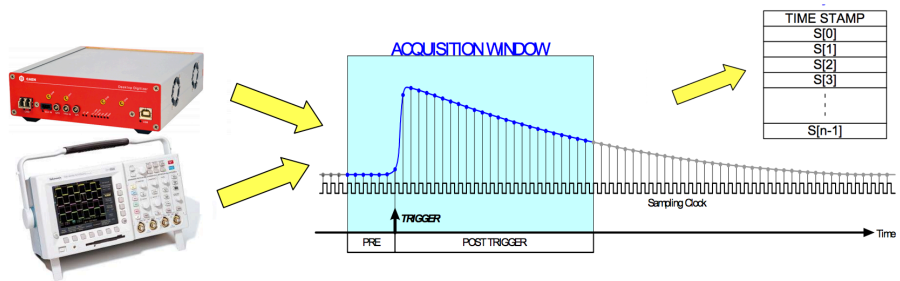


A digital system replaces the above with:



Principle of digital spectroscopy

Just like a digital oscilloscope, an analogue signal is sampled at regular intervals to produce a digital approximation of the signal



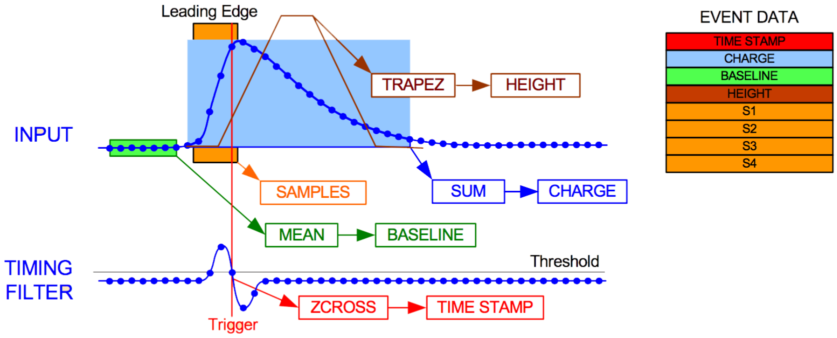
Separation of sample points is 1/clock frequency.

E.g. 100 MHz clock give 1 sample every 10 ns

Higher clock speed gives better representation of continuous signal

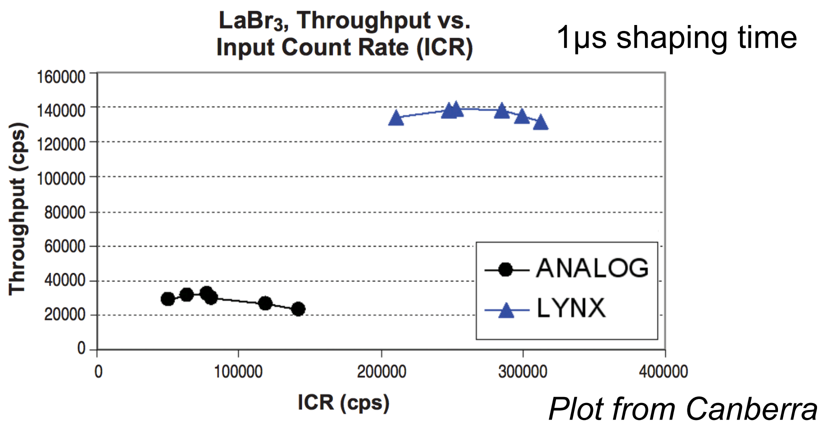
Principle of digital spectroscopy

Once a digital copy of the pulse has been made, algorithms can be run (both online and offline) to extract energy, timing and other useful information that is not easily obtainable using analogue electronics



Why digitise signals? - Throughput

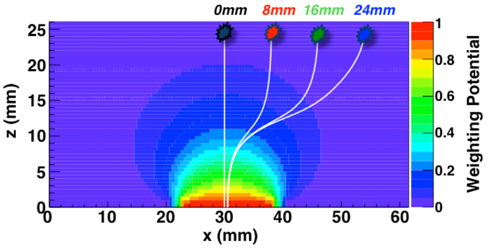
- Higher throughput compared to analogue systems – From figure below;
  - Analogue max throughput ~ 32,000 cps
  - Digital max throughput ~ 140,000

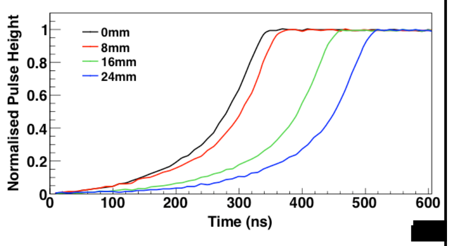


Plot from Canberra

Why digitise signals? - PSA

- Pulse Shape Analysis
  - Information about the interaction is often contained in the shape of the detector pulse
    - Type of radiation depositing energy
    - Position of interaction within the detector

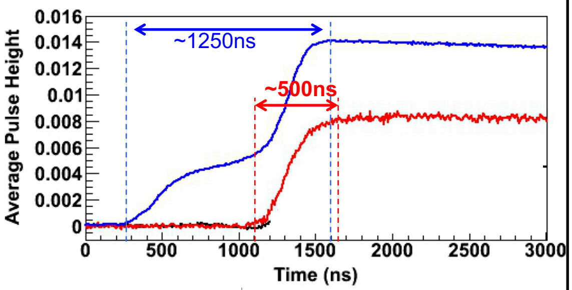


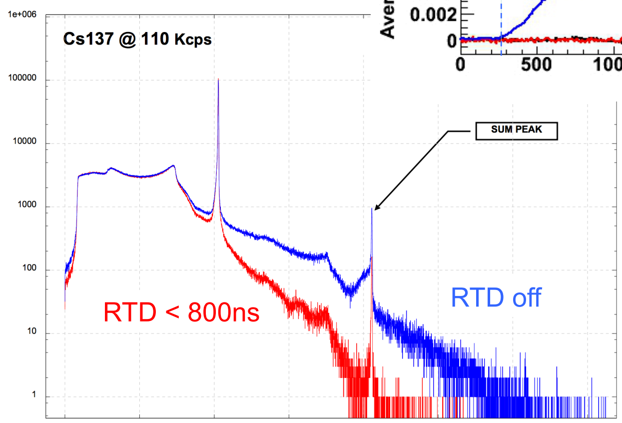


Why digitise signals? - RDT

Rise Time Discrimination

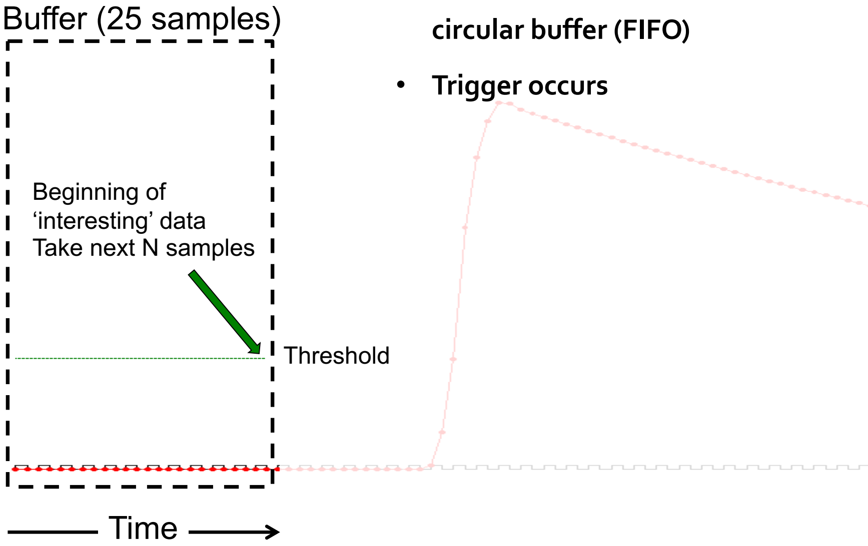
- Reject pulses with longer than expected rise times
- And/or, differentiate between incoming radiation types





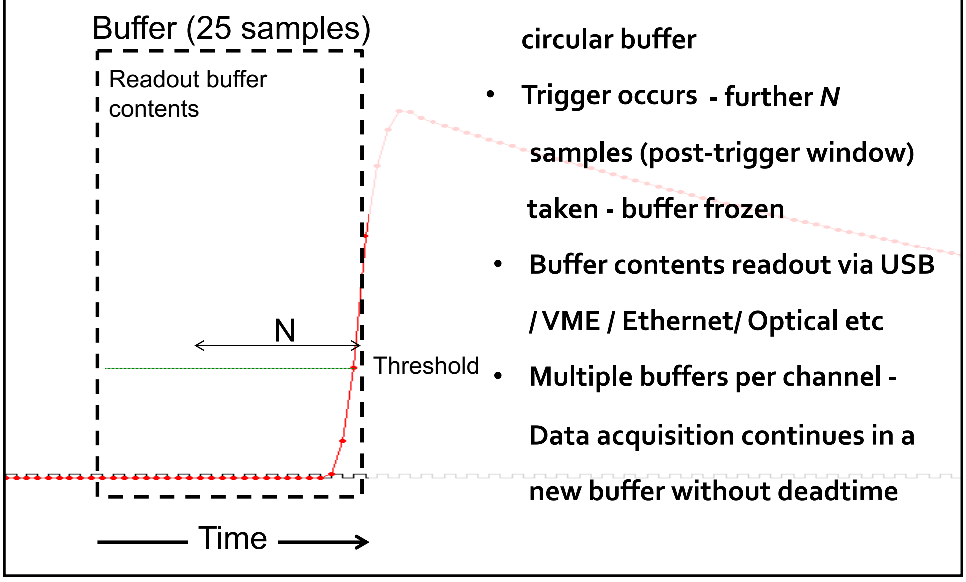
Spectra from Caen

Signal digitisation



- **Data continuously read into circular buffer (FIFO)**
- **Trigger occurs**

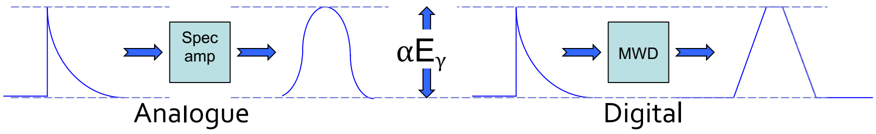
Signal digitisation



- **Data continuously read into circular buffer**
- **Trigger occurs - further *N* samples (post-trigger window) taken - buffer frozen**
- **Buffer contents readout via USB / VME / Ethernet/ Optical etc**
- **Multiple buffers per channel - Data acquisition continues in a new buffer without deadtime**

Energy Filter - Moving Window Deconvolution

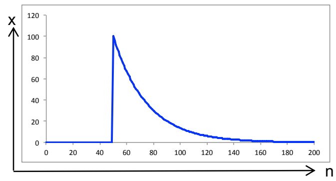
- Digital equivalent of analogue Gaussian shaper (CR-RC circuit)
- Transforms 'fast' preamp signal into more suitable shape for energy determination



- Duration of trapezoid is much shorter than exponential decay
  - less dead-time / pileup

Energy Filter - Moving Window Deconvolution

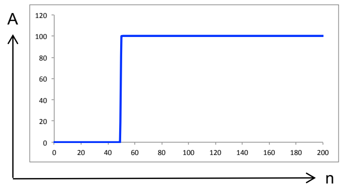
- The MWD filter has 3 stages – example with 'perfect' data
  - It starts with the initial digitised signal from the pre-amp



Function

$x[n]$

- **Stage 1** transforms this from a continuous discharge signal into a transistor reset (step) signal by removing the exponential tail

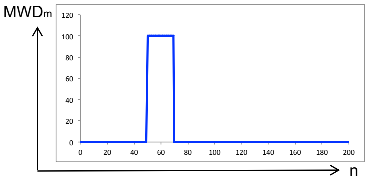


Function (τ = decay constant)

$$A[n] = x[n] - (1 - (1/\tau))x[n-1] + A[n-1]$$

Energy Filter - Moving Window Deconvolution

- **Stage 2** differentiates the output of stage 1 to give a square pulse

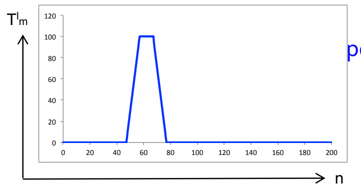


Function (parameter ***m*** defines width)

$$MWD_m[n] = x[n] - x[n-m] + \frac{1}{\tau}\sum_{k=n-m}^{n-1} x[k]$$

$$= A[n] - A[n-m]$$

- **Stage 3** runs a moving average over the output of stage 2 to smooth out noise and gives a trapezoidal shape



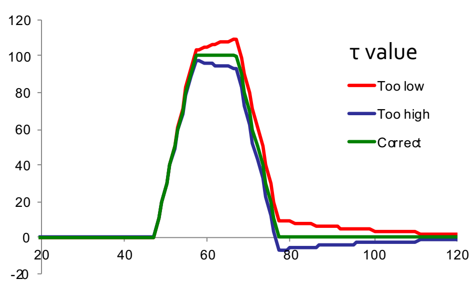
Function (parameter ***l*** defines trap' pe)

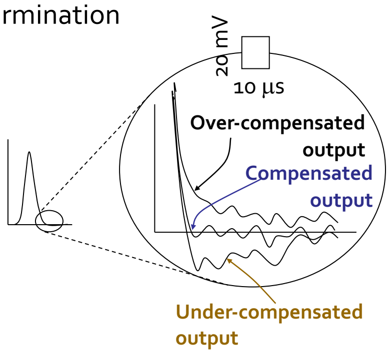
$$T_m^l[n] = MA_l(MWD_m[n])$$

$$= \frac{\left(\sum_{k=n-l}^{n-1} MWD_m[n]\right)}{l}$$

Energy Filter - Moving Window Deconvolution

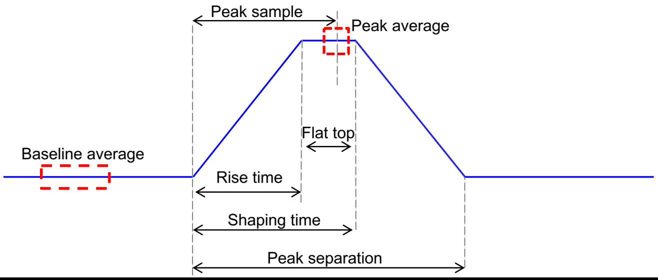
- The decay constant, τ, works in a similar way to the pole zero correction in an analogue setup
- Must be set correctly to give the trapezoid a flat top
  - – essential for proper energy determination





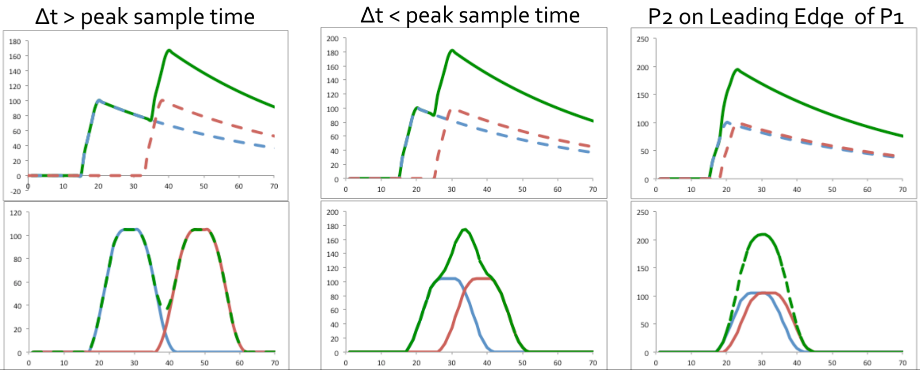
Energy Filter - Moving Window Deconvolution

- In previous equations: l = Rise time / Peaking time, m = Trapezoid flat top, $m + l$ = Shaping time, $2l + m$ = Peak separation
- Peak sample is the point at which the height of the trapezoid is calculated
- Signal height = (Peak average – Baseline average) -> proportional to energy
- In analogy with analogue shaping time, choosing the optimum trapezoid parameters is a trade-off between good energy resolution and high dead-time



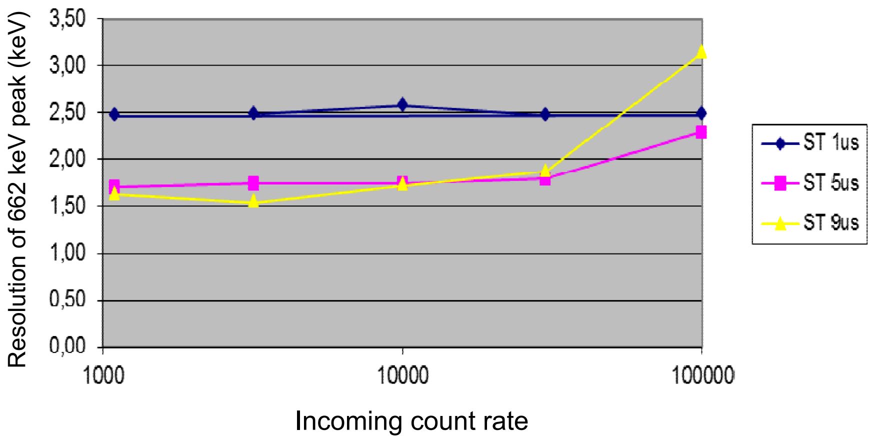
Energy Filter - Moving Window Deconvolution

- The time difference between 2 pulses = Δt
  - If Δt > peak sample time - 2 pulses can be resolved ok
  - If Δt < peak sample time - 2 pulses cannot be resolved, pileup identified
- If P2 on Leading Edge of P1 - 2 pulses cannot be resolved, pileup not identified

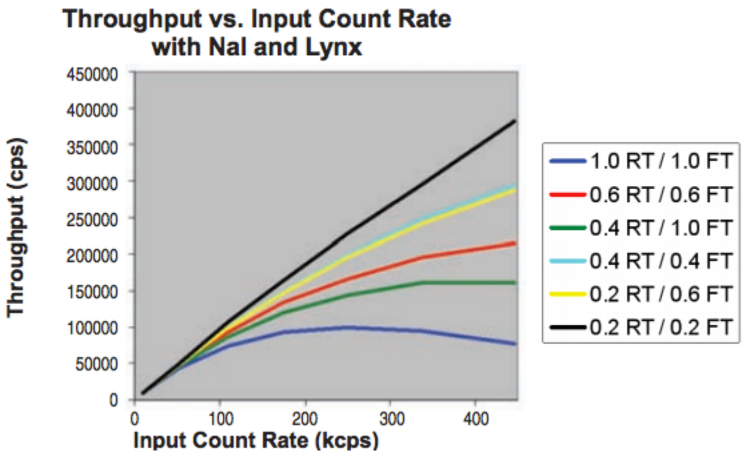


Energy Filter - Moving Window Deconvolution

Energy resolution v's count rate for various shaping times

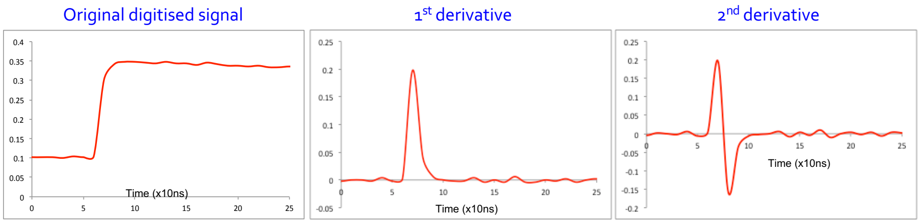


Energy Filter - Moving Window Deconvolution



Digital timing filter

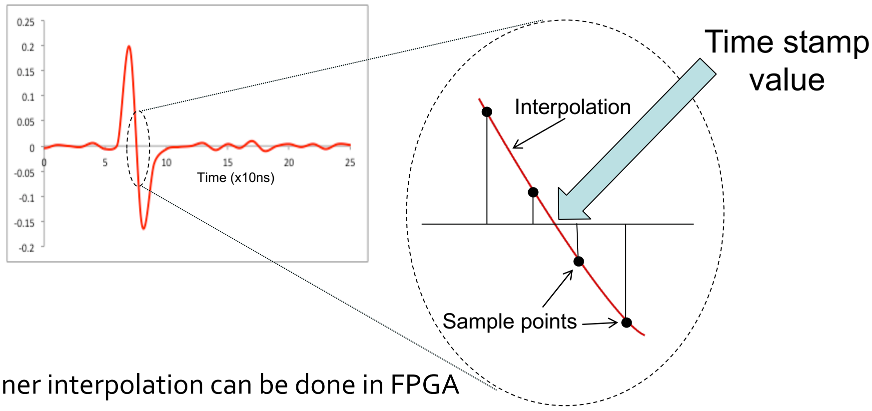
- Need to be able to determine when the signal was generated
- Analogy with analogue CFD



- 1st derivative removes baseline offset
- Zero crossing of the 2nd derivative gives the timing, independent of signal amplitude

Digital timing filter

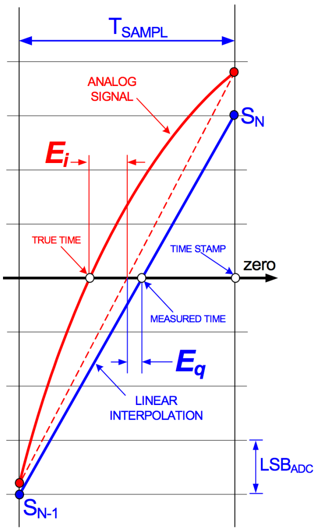
- Interpolation between samples can improve timing resolution



- Liner interpolation can be done in FPGA
- More complex interpolation generally done offline as computationally intensive + needs to be tailored to application

Digital timing filter

Timing errors



- Quantisation error E_q (like walk in analogue)
- Interpolation error E_i

Rise Time > 5xTs

Approximation to linear is ok $E_i << E_q$

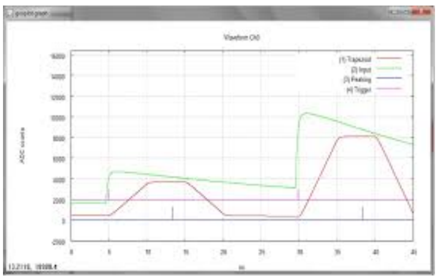
Rise Time < 5xTs

Approximation to linear is poor $E_i > E_q$

Optimum Rise Time = 5 x Ts

Digitiser types

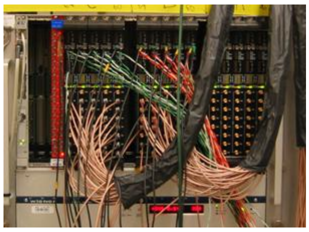
- **Standard commercial products – (practical 2)**
  - **1-box spectroscopy**
  - **Usually 1-2 channels**
  - **Provides low and high voltage**
  - **Usually records only energy and timing**
  - **Traces used only for diagnostics**



Canberra Lynx
Ortec dspec
Caen DT5780

Digitiser types

- **Research grade – (practical 3)**
  - **Multi channel – modular**
  - **Records partial traces**
  - **Programmable FPGA**
  - **Custom software**



Agata, Gretina, Lyrtech, v1724, TIG10, etc

Digitiser specifications

- **Clock frequency -** determines how often the analogue input signal is sampled. Faster clock speed = more samples = better digital signal
- **Nº Bits** – Higher number of bits -> better resolution
- **Dynamic range** – Size of the signal the digitisers can process
- **FPGA size** determines the number of and complexity of algorithms / calculations that can be done on the cards themselves
- **Bandwidth** determines how many events per second can be processed

Usually a compromise between all of these parameters and cost

Specifications

Commercially available CAEN digitisers

Model [1]	Form Factor	N. of ch. [4]	Max. Sampling Frequency (MS/s)	N. of Bits	Input Dynamic Range (Vpp) [4]	Single Ended / Differential Input	Bandwidth (MHz)	Memory (MS/ch) [4]	DPP firmware [5]
x724	VME	8	100	14	0.5 / 2.25 / 10	SE / D	40	0.5 / 4	PHA
	Desktop/NIM	4 / 2				SE			
x720	VME	8	250	12	2	SE / D	125	1.25 / 10	CI, PSD
	Desktop/NIM	4 / 2				SE			
x721	VME	8	500	8	1	SE / D	250	2	no
x731	VME	8 - 4	500 - 1000	8	1	SE / D	250/500	2/4	no
x730	VME	8	500	12	2	SE / D	250	1.25 / 10	PSD
	Desktop/NIM	4 / 2				SE			
x751	VME	8 - 4	1000 - 2000	10	1	SE / D	500	1.8 / 14.4 - 3.6 / 28.8	PSD
	Desktop/NIM	4 - 2				SE			
x761	VME	2	4000	10	1	SE / D	TBD	7.2 / 57.6	no
	Desktop/NIM	1				SE			
x740	VME	64	62.5	12	2 / 10	SE	30	0.19 / 1.5	no
	Desktop/NIM	32							
x742	VME	32+2	5000 [2]	12	1	SE	600	0.128 / 1 [3]	no
	Desktop/NIM	16+1							

Multi-Channel acquisition

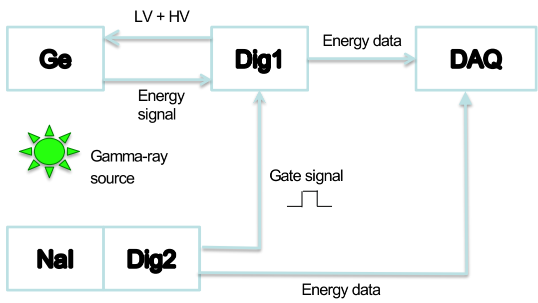
Often need to process data from multiple detectors / channels at once

- 1 digitiser per channel
- Common clock signal or synchronisation signal to align clocks on multiple digitisers
- Time stamp individual digitiser data with common / aligned clock
- Common trigger logic to decide which channels to write out, either
  - Hardware gating – more efficient (lower data rate)
  - Software gating – more flexible

Coincidence – Hardware gated

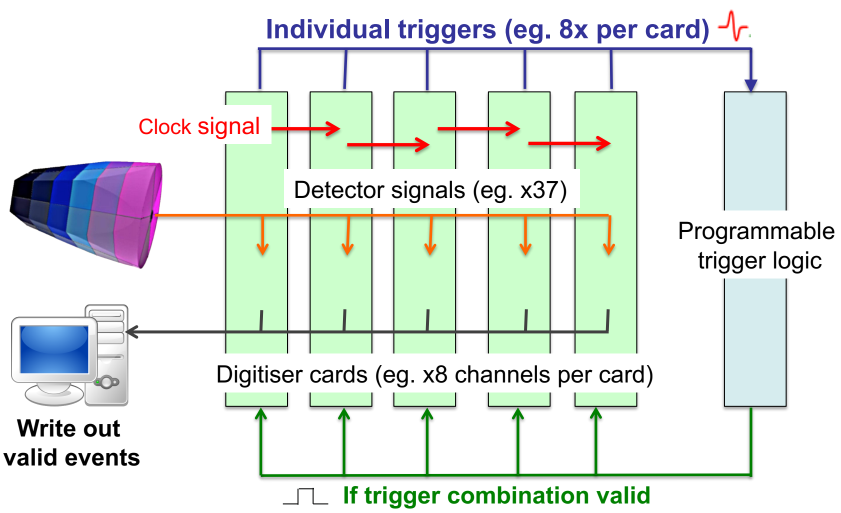
Hardware gated coincidence

- 1st digitiser generates a gating signal when it triggers off a 'useful' event. 2nd digitisers output data only when it's trigger is within the gating signal. The width of the gate determines the resolving time.
- DAQ analyses coincident / anticoincident events



Coincidence – Hardware gated

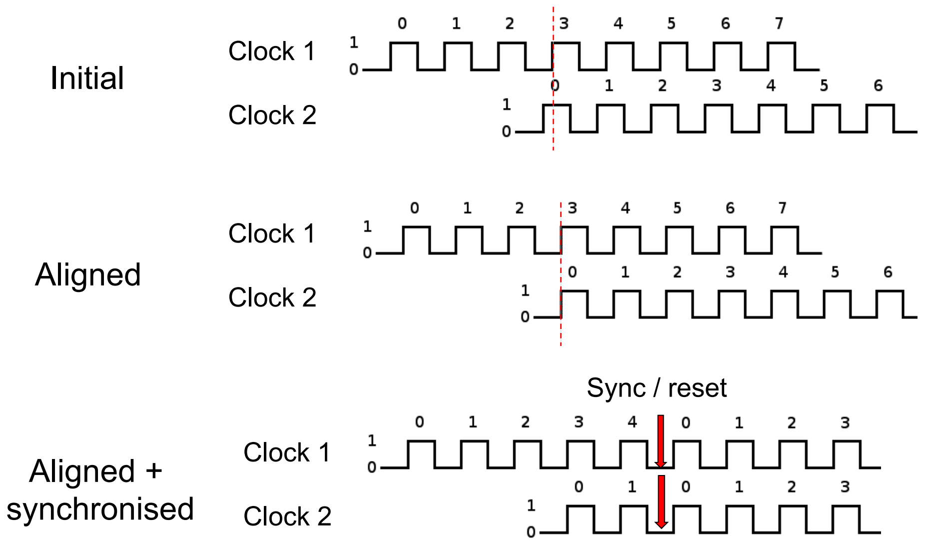
Multichannel system - Programmable hardware gate



Coincidence – Software gated

- The signals from detector preamplifiers are digitalized and recorded event by event with amplitude and timestamp
- Offline (or online) analysis and spectral reconstruction can be performed on the selected coincident / anticoincident event
- Comparing with analogue coincidence/anticoincidence counting system, the software gated data analysis has higher flexibility of data manipulation with coincidence criteria between different detectors
- Crucial that the time stamps from different channels are correlated
- Number of timestamp bits determine how wide coincident window can be. E.g. for a 100Mhz clock
  - 16 bit = 655 μs, 32 bits = 42.9 s, 48 bits = 32.6 days

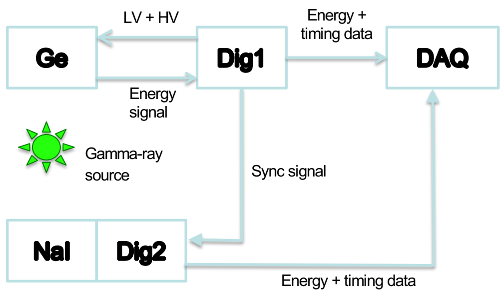
Clock alignment



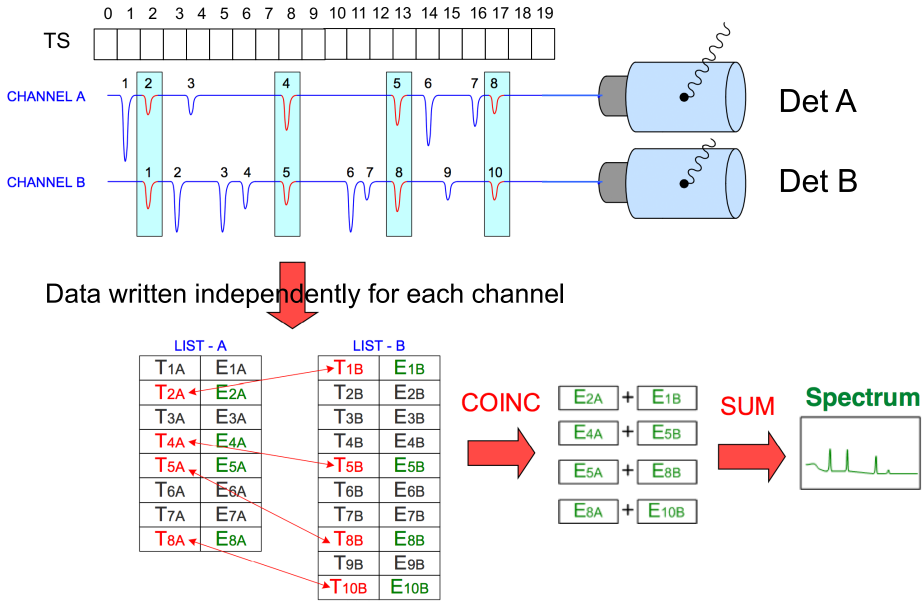
Coincidence – Software gated

Software gated (time stamp comparison)

Coincident events identified by comparing time stamp values in software. Relies on the clocks in the digitisers being synchronised / aligned. 1st digitiser takes role of 'master' and distributes clock reset signal to other (slave) digitisers.

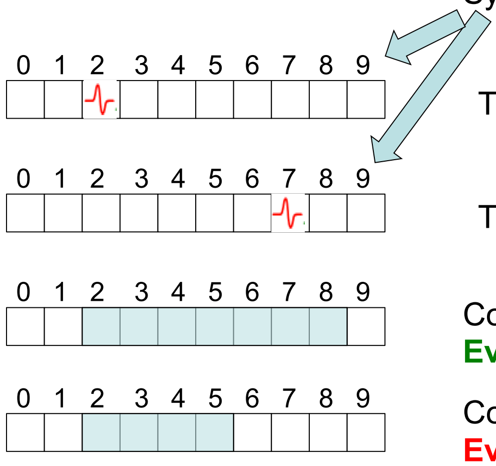


Coincidence – Software gated



Coincidence – Software gated

Synchronised clocks (100 Mhz)



TS of trigger1 = 2 (20 ns)

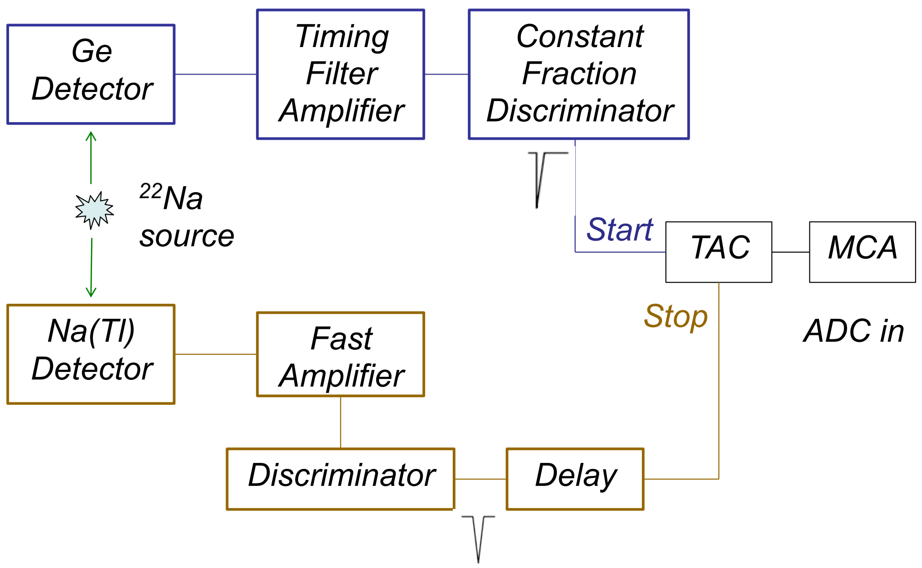
TS of trigger2 = 7 (70 ns)

Coincidence window = 70 ns
Events are in coincidence

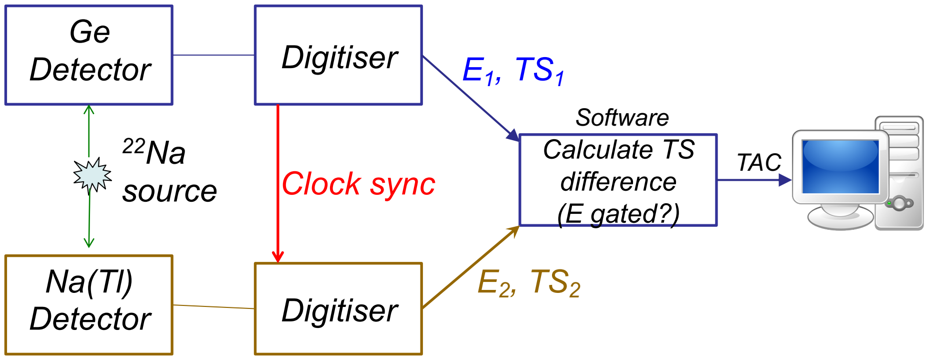
Coincidence window = 40 ns
Events not in coincidence

ΔT = TS2 – TS1

TAC Measurement - Analogue



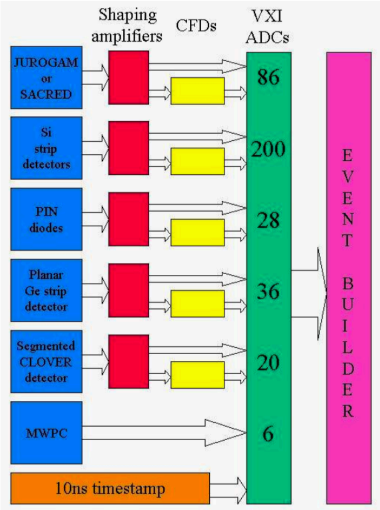
TAC Measurement - Digital



Total Data Readout (TDR)

- Data taken in Jyvaskyla relies on the Total Data Readout (TDR) principle
- No hardware trigger
- Data from all systems is written out independently as an unstructured stream
- Every event is time stamped with a global time stamp (10Mhz clock) and tagged with a detector / channel ID
- Reconstruct 'events' based on software gates – more flexible
- Correlate prompt and delayed events
- High rates without trigger deadtime issues

Total Data Readout (TDR)



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